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Tantalum oxide thin films for microelectronic applications

Fang-Xing Jiang

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Fang-Xing Jiang

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for Microelectronic Applications

by

Fang-Xing Jiang

A thesis submitted in partial fulfillment of
the requirements for the degree of

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at the Rochester Institute of Technology

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Abstract

There is a critical demand for new dielectric films having higher dielectric constants, higher dielectric strengths and lower leakage currents for applications such as charge storage capacitors for DRAMs in ULSI and low-inductance decoupling capacitors for the control of simultaneous switching noise (SSN) in high-speed switching ULSI chips. Among these candidates for insulators, tantalum pentoxide has received considerable attention. As earlier as in the 1960's, tantalum oxide has been used as the dielectric in discrete capacitors. Recently, several papers have been reported on the electrical properties of Ta_2O_5 films grown by various techniques. It has been reported that the electrical properties, e.g. dielectric constant, leakage current, dielectric strength as well as the nature of the Ta_2O_5/Si interface, are extremely sensitive to the annealing conditions. At the present time, however, the role of the as-deposited Ta_2O_5/Si interface is not fully understood.

In the present study, a two-step process, consisting two separate depositions and annealing, has been developed to improve the physical and electrical characteristics of reactivity sputtered Ta_2O_5 films. The reactive ion etching (RIE) selectivity of Ta_2O_5 to Si, SiO_2 and Ta in CHF_3, CF_4 and SF_6 with fractions of O_2, H_2 and Ar has been investigated for IC process applications.

The tantalum oxide films were deposited on Si wafers by reactive DC sputtering. The films were characterized for thickness and refractive index using an ellipsometer and their phase was identified using an X-ray diffractometer. The annealing effect on Ta_2O_5 in

oxygen ambient at 800°C shows that the Ta_2O_5 films crystallize into an orthorhombic phase, condensed with a decrease of thickness and an increase of refractive index. Various capacitor configurations, such as MIM (Al/Ta_2O_5/Al) and MIS (Al/Ta_2O_5/p-Si, Al/Ta_2O_5/n-Si and Al/Ta_2O_5/n+-Si), were fabricated to study the nature of Ta_2O_5/Si interface and the I-V and C-V characteristics. The as-deposited Ta_2O_5 film on p-type Si substrate can sustain an electric field of 3 MV/cm at a current density of 1 μA/cm2 in the accumulation mode, which is an order higher than that on n-type substrate. The value of apparent dielectric constant of as-deposited Ta_2O_5 film estimated from the Al/Ta_2O_5/Al capacitor is 16, however, the value varies from 6 to 10 in MIS capacitors. This shows a evidence strongly that there is a substrate sensitivity for tantalum oxide films. As a result of the two-step process, the dielectric constant of Al/Ta_2O_5/n+-Si capacitor increases to 21. This value is considerably close to 24 for bulk Ta_2O_5.

To investigate the RIE selectivity of Ta_2O_5 to Ta, Si and SiO_2, the Ta_2O_5 film was deposited onto a wafer with three other films, DC sputtered Ta, LPCVD polysilicon, and thermally grown SiO_2. It is revealed that in SF_6 with various fractions of 20% hydrogen or argon, the Ta_2O_5 film shows extremely low etch rate as compared with Si, Ta and SiO_2, and in CF_4 with various fractions of 30% hydrogen or oxygen, the Ta_2O_5 film shows a lower etch rate. However, in CHF_3 the etch rates of Si and Ta_2O_5 are comparable.

The absorption spectrum of deposited tantalum oxide films was also measured. This material can be used for phase shift and attenuation masks, sunglasses and light filters. The as-deposited tantalum oxide films show a high absorbency peak at 217 nm and an additional small peak at 416 nm with two subpeaks at 286 and 510 nm using

spectrophotometer. The high peak becomes broadened and the long wavelength side of the small peak is shifted to short wavelength through annealing. A model of free volume like defect and oxygen vacancy like defect is proposed to explain the change of the absorbency spectrum.

Chapter 1. Introduction

1.1. High Dielectric Insulator for Next Generation of DRAM's Storage Capacitor

Over the last several years, tantalum pentoxide (Ta_2O_5) thin films have received much attention as a chip-integrated high permittivity, high breakdown strength dielectric for storage capacitors for ULSI DRAM's. In 1993, the Watkins-Johnson Company[1] reported a 64 Mbit DRAM using tantalum oxide instead of silicon oxide. In 1994, a Japanese company, NEC corporation[2], and a Korea company, Samsung Electronics Corporation[3], both reported a 1 Gbit DRAM of Ta_2O_5 capacitor.

To scale down VLSI's, it is necessary to reduce the device size. In the development of DRAM's, three-dimensional device structures such as trenched or stacked capacitors have been used to shrink the memory cell area. Other way to reduce the device size is to reduce the thickness of the dielectric layer in the capacitor because of the requirement for constant capacitance. Due to the limitation of electric strength, the reduction of the dielectric layer will require a reduction of operating voltage. In addition, the reduction of operation voltage for low-power operation will require a further increase in capacitance. Generally, the cell area decreases exponentially as the density of DRAM's increases. Consequently, capacitance density, defined as the capacitance divided by the projection area of the storage node, should increase with the DRAM's density as shown in Fig. 1.1.1 [3]. The capacitance density of 145 and 330 $fF/\mu m^2$ is required for the 1 Gbit

and 4 Gbit DRAM, respectively, for a target capacitance of 25 fF/cell. However, conventional films such as SiO_2/Si3N4 films on polysilicon have reached their physical limits in terms of thinning. This is because direct tunneling current greatly increases below the effective SiO_2 film thickness of 5 nm. A requirement of high dielectric insulator is necessary for the next generation, high density DRAM's. The Ta_2O_5 film is a good candidate because of high dielectric constant, stable electric characteristics and easy fabrication.

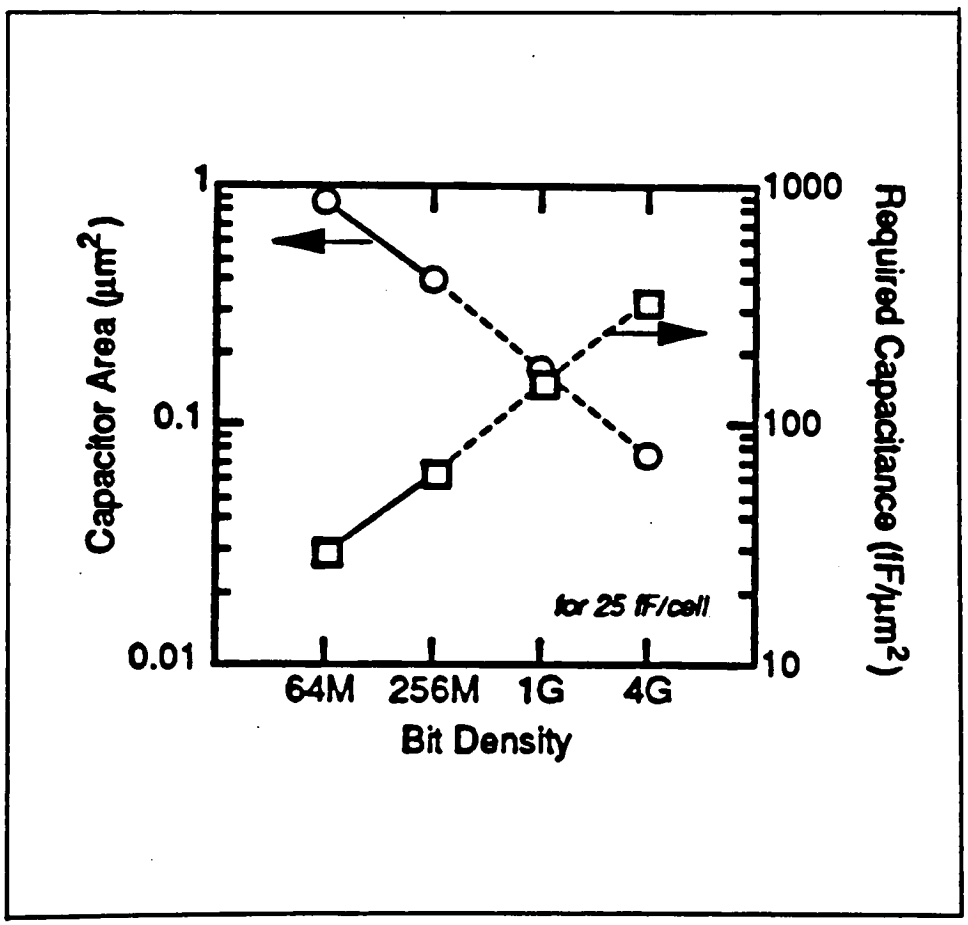


Fig. 1.1.1. Capacitor area and capacitance density as a function of DRAM bit density from reference [3]

1.2. Physical Characteristics of Dielectric[4]

1.2a. Dielectric Constant (Permittivity)

A capacitor, connected to a potential V with two plates of an area A in a distance d in vacuum, stores a charge

$$Q = C_o V \qquad (1.2.1)$$

or

$$C_o = \varepsilon_o A/d \qquad (1.2.2)$$

where C_o is the vacuum (or geometrical) capacitance of the condenser and ε_o designates the permittivity or dielectric constant of vacuum.

When filled with some dielectric material, the condenser increases its capacitance to

$$C = \varepsilon C_o = \varepsilon \varepsilon_o A/d \qquad (1.2.3)$$

where ε is the dielectric constant of the filled material. The higher the dielectric material filled in the space of the capacitor, the larger the capacitance. In other words, the higher the dielectric, the smaller the capacitor area for same capacitance. That is why the semiconductor industry searches the high dielectric for IC design in order to increase the high device density.

1.2b. Refractive Index

Let us consider an electromagnetic wave traveling through a medium. In vacuum, the wave travels with the velocity of light, c, and the wavelength λ_0 is given by

$$c = \lambda_0 \nu = 1/(\varepsilon_0 \mu_0)^{1/2} \qquad (1.2.4)$$

where ν is the wave frequency. In other media, the wavelength normally shortens and the phase velocity slows down. The ratio of the wavelength or phase velocity in vacuum to that in the dielectric designates the index of refraction of the dielectric medium as

$$n = \lambda_0/\lambda = c/v \qquad (1.2.5)$$

where v is the wave velocity in the dielectric. For a loss-free medium, this equation simplifies to

$$n = (\varepsilon\varepsilon_0 \mu / \varepsilon_0 \mu_0)^{1/2} \qquad (1.2.6)$$

If, in addition, the magnetization can be neglected ($\mu=\mu_0$), the well-known Maxwell relation results as :

$$n^2 = \varepsilon \qquad (1.2.7)$$

This relation has been abused frequently in predicting static dielectric constants from optical refraction data. Actually, it states that the square of the index of refraction of a nonabsorbent and nonmagnetic material is equal to the relative permittivity at that frequency. Generally, the larger the refractive index, the higher the dielectric constant. So knowing the change of refraction index is a way to know about the change of dielectric. Keep in mind, this relationship has been used to discuss the characteristics of the Ta_2O_5 film frequently in the present study.

1.3. Electrical Characteristics of Dielectric[5]

The leakage current and the breakdown voltage are important electrical characteristics of the dielectric and they limit the applications of dielectric materials. Although dielectrics are defined as materials which do not allow current to flow under DC voltage. However, in fact, any dielectric has a finite large resistivity. For a dielectric, a current vs. voltage characteristics exhibit three regions as shown in Fig.1.3.1. In the first region, the current varies in an ohmic manner, rising linearly with increasing voltage, up to values not exceeding a microampere; in the second region, the current remains almost

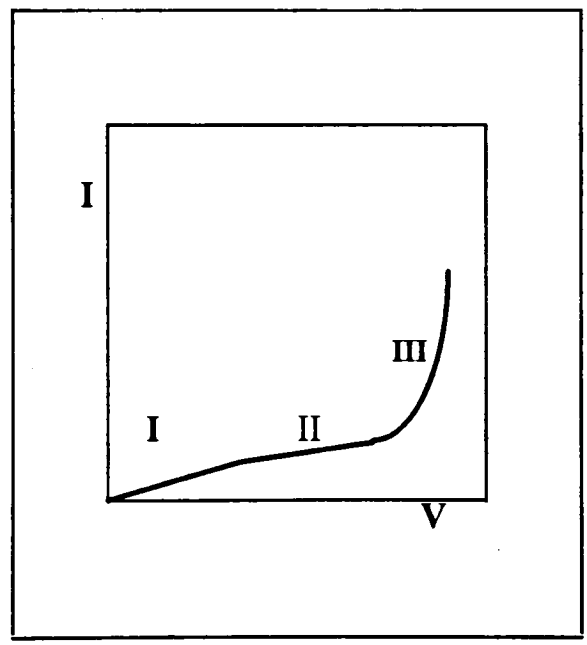


Fig. 1.3.1. Three regions of leakage current and breakdown of dielectric

constant with the voltage increase, which is a saturation region. The current in the first two regions is defined as the leakage current. In third region, the current rises steeply

while the voltage is above a certain value which is referred to as the breakdown voltage. It is important to keep in mind that the mechanism of leakage current is different from that of breakdown voltage even though they are shown on the same curve.

1.3a. Leakage Current

There are two mechanisms of electrical conduction in dielectrics, which are distinguished by the type of carriers : ionic conduction and electronic conduction.

Ionic conduction occurs either through the migration of positive and negative ions originating from the substrate and the impurities, or through the motion of ions in vacancies under an external electric field. This electrical conductance is influenced by the thermal treatment of dielectrics, even pure ones. Thus, the conductance depends on the cooling rate from high temperature. For slow cooling the remaking of the lattice can occur by the migration of interstitials to vacancies, recombination of Schottky defects or migration of vacancies to the surface or along dislocation channels. However, a fraction of the vacancies freeze on quenching or rapid cooling. That is why we need to anneal samples after sputtering and chemical vapor deposition in order to obtain a low leakage current.

Electronic conductance is determined by the motion of free electrons and holes that originate in (a) the generation of free electrons in conduction band and (b) the generation of additional electrons or holes following the generation of vacancies by a chemical reduction process or by a controlled doping. In other words, the impurities in dielectrics can contribute to the leakage current. Free electrons may be induced by internal

photoelectric effect, by injection from the electrode at the metal-dielectric contact (Schottky emission), or by ionization of traps (Frenkel effect). The generation of free electrons by thermal excitation or band-band tunneling in the presence of a strong electric field may be neglected since the band gap, i.e. the forbidden interval, of dielectric is wider than 5 eV.

1.3b. Breakdown Voltage

Breakdown strength is a function of many parameters such as the temperature, the rate of increase of the applied voltage, the sample thickness and the crystalline direction. It is also strongly influenced by the purity and homogeneity of the dielectric materials, the atmosphere, the type and geometry of electrodes. Typically, it is accepted that there are three types of breakdown: (a) thermal breakdown, (b) intrinsic breakdown and (c) avalanche breakdown.

Thermal breakdown is caused by conduction current that may heat up the dielectric locally either by the Joule effect or by relaxation phenomena at a rate that is higher than the dissipation of heat, causing the temperature to rise. Due to the low thermal conductivity of dielectrics, the amount of locally produced heat is larger than that dissipated. The local accumulation of heat may cause either the thermal generation of free charges by transition from deep levels and band-band transition, or the local melting although the sample temperature is well below the melting point of dielectrics. Local chemical decomposition of dielectrics may also occur. All these phenomena, separate or together, lower the stiffness and favor breakdown.

Intrinsic breakdown is related to the existence of free electrons. It takes place in very short times and sometimes at room temperature. It also does not depend on the shape and dimensions of samples and electrodes. Of the possible sources of migrating electrons, two important sources have been considered: (a) traps of electrons related to donors, impurities, irregular layers and dislocations which possess a ground state and several unoccupied exited states below the conduction band and (b) transition for free electrons by band-band tunneling.

Avalanche breakdown is similar to the breakdown of gases by electrical discharge and causes the lattice destruction. In the case of conduction electrons, it is agreed that there are electron-lattice collisions with partial energy transfer. These collisions are numerous as the concentration of the electrons increases in the avalanche. The local energy accumulation may produce a breakdown of the lattice, which may be understood as a local explosion caused by electrostatic repulsion.

1.4. Optical Characteristics of Materials[6]

In terms of solid state physics, the color and the transparency or opaqueness of materials represent the band structures and the bonds of molecules and compounds. The tool to study optical characteristics is optical spectroscopy. The mechanism of optical spectroscopy is based on the Bohr-Einstein frequency relationship

$$\Delta E = E_2 - E_1 = h\nu \qquad (1.4.1)$$

This relationship links the energy states of the materials with the frequency ν of the electromagnetic radiation. In spectroscopy, it is appropriate to use the wavenumber or the wavelength instead of frequency. Absorbed or emitted radiation of wavenumber or wavelength can thus be assigned to specific energy level differences of energy bands and compound bond.

In a spectrophotometer, nowadays more usually termed a spectrometer or disperse spectrometer, the measuring light is split up (dispersed) into its constituent wavelengths by a monochromator, using a prism or grating. With a deuterium lamp for the UV region and a tungsten lamp for the VIS region, these instruments allow the continuous variation of the measurement wavelength over the whole spectral region. Most instruments cover the range 190 to 900 nm.

1.5. Characteristics of Bulk Tantalum Pentoxide

All the characteristics of bulk tantalum pentoxide are good references for us to understand the deposited tantalum oxide films. There is the information about phase diagram, dielectric constant and X-ray ASTM card from some handbooks.

1.5a. Binary Phase Diagram of Tantalum and Oxygen

In 1972, Jehn and Olzi reported the high temperature solid-solubility limit and phase studies in the system tantalum-oxygen and obtained a binary phase diagram [7][8]. This diagram is shown in Figure 1.5.1. The Ta_2O_5 has an α phases: α-Ta_2O_5 with <71.4 at% of O.

1.5b. Dielectric Constant

The dielectric constant has been listed in the Handbook of Chemistry and Physics [9] as

Ta_2O_5	α-phase	$\varepsilon_{11} = \varepsilon_{22} = 30$	77K
		$\varepsilon_{33} = 65$	
	β-phase	$\varepsilon = 24$	292K

Two phase, α-phase and β-phase, were defined related to the temperature. So the definition of phase for dielectric constant in the Handbook of Chemistry and Physics is different from that in the binary-phase diagrams.

1.5c. Crystal Structure of Tantalum Pentoxide

The structure of tantalum pentoxide at low temperature is orthorhombic. It is an ASTM card of No:8-255 as shown in Figure 1.5.2.

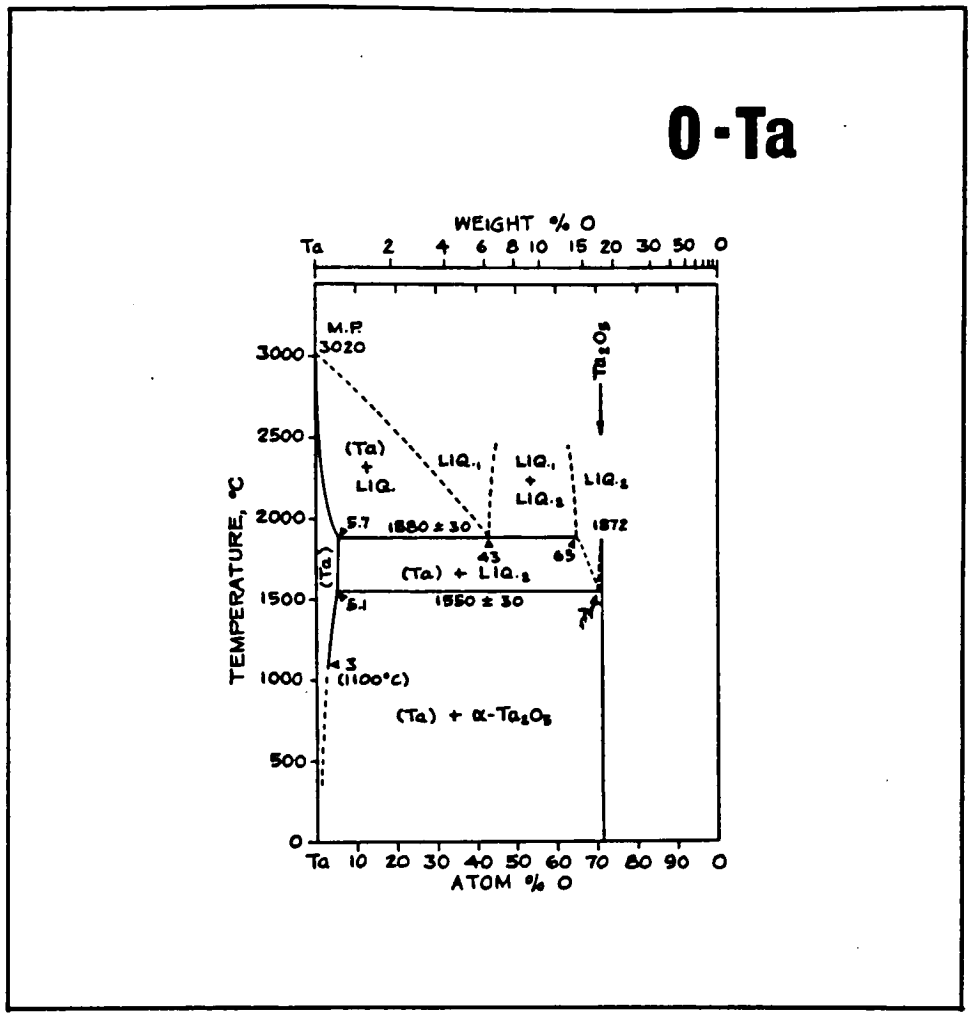
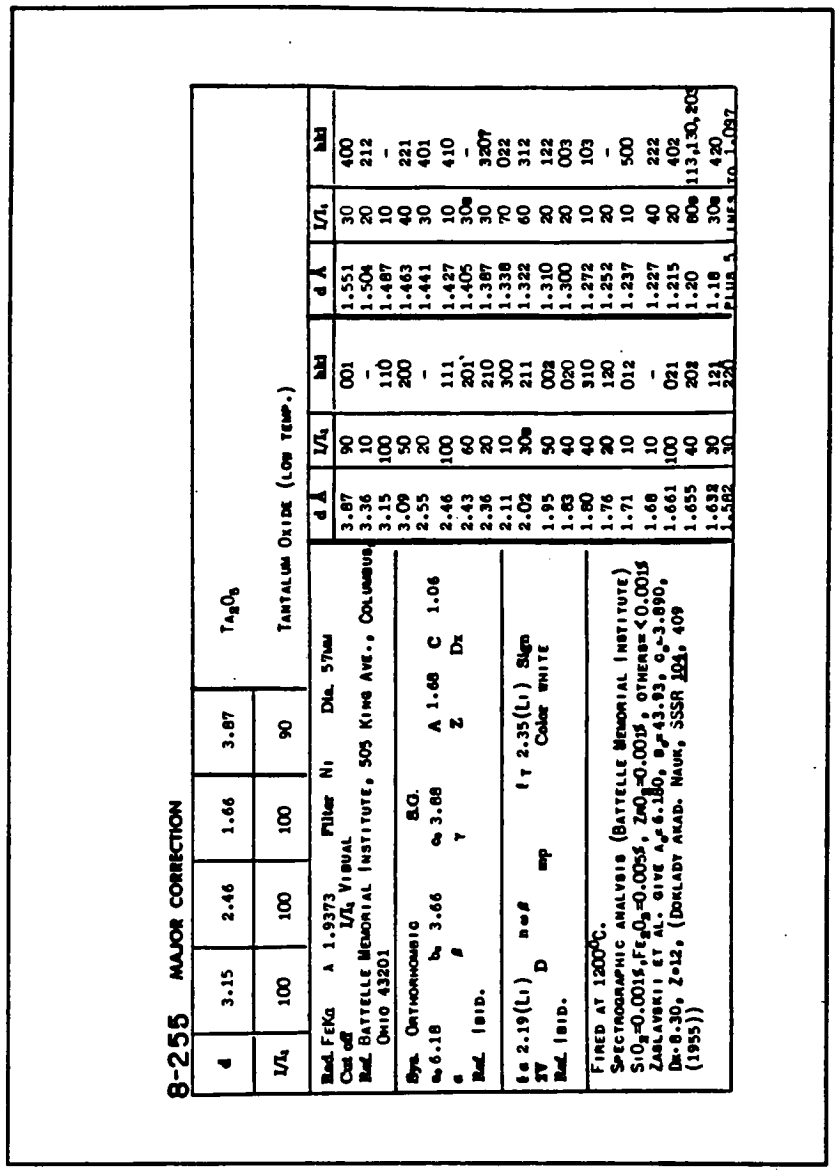


Fig. 1.5.1. Binary phase diagram of tantalum oxygen from reference [7,8]



8-255 MAJOR CORRECTION

d	3.15	2.46	1.66	3.87
I/I1	100	100	100	90

Ta_2O_5

Tantalum Oxide (Low Temp.)

Rad. FeKα λ 1.9373 Filter Ni Dia. 57mm
Cut off I/I1 Visual
Ref. Battelle Memorial Institute, 505 King Ave., Columbus, Ohio 43201

Sys. Orthorhombic S.G.
a 6.18 b 3.66 c 3.88 A 1.68 C 1.06
α β γ Z Dx
Ref. Ibid.

ε 2.19(Li) nεβ ω 2.35(Li) Sign
2V D mp Color White
Ref. Ibid.

Fired at 1200°C.
Spectrographic analysis (Battelle Memorial Institute) SiO_2=0.0015, Fe_2O_3=0.0055, ZrO=0.0015; others=<0.0015
Zablavskii et al. give a_o=6.180, b_o=43.93, c_o=3.890, Dx=8.30, Z=12, (Doklady Akad. Nauk, SSSR 104, 409 (1955))

d Å	I/I1	hkl	d Å	I/I1	hkl
3.87	90	001	1.551	30	400
3.36	10	-	1.504	20	212
3.15	100	110	1.487	10	-
3.09	50	200	1.463	40	221
2.55	20	-	1.441	30	401
2.46	100	111	1.427	10	410
2.43	60	201	1.405	30b	-
2.36	20	210	1.387	30	3207
2.11	10	300	1.338	70	022
2.02	30b	211	1.322	60	312
1.95	50	002	1.310	20	122
1.83	40	020	1.300	20	003
1.80	40	310	1.272	10	103
1.76	20	120	1.252	20	-
1.71	10	012	1.237	10	500
1.68	10	-	1.227	40	222
1.661	100	021	1.215	20	402
1.655	40	202	1.20	60b	113,130,403
1.638	20	121	1.18	30b	420
1.582	30	220	Plus 5 lines to 1.097		

Fig.1.5.2. X-ray ASTM card of tantalum pentoxide.

1.6. Theory of the MOS Capacitor

Two kinds of capacitors, the MOS capacitor and the DRAM's storage charge capacitor, are introduced in this section. The device physics and structure of capacitors will be discussed.

1.6a. MOS Capacitor[10]

The heart of the MOSFET is a metal-oxide-semiconductor structure known as a MOS capacitor. The energy bands in the semiconductor near the oxide-semiconductor interface bend as a voltage is applied across the MOS capacitor. The position of the conduction and valence bands relative to the Fermi level at the oxide-semiconductor interface is a function of the MOS capacitor voltage. The operation and characteristics of the MOSFET are dependent on this inversion and the creation of an inversion charge density at the semiconductor surface.

A great deal of information about the MOS device and the oxide-semiconductor interface can be obtained from the capacitance versus voltage or C-V characteristics of the device.

First we will consider the ideal C-V characteristics of the MOS capacitor and then discuss some of the deviations that occur from these idealized results. We will initially assume that there is zero charge trapped in the oxide and also that there is no charge at the oxide-semiconductor interface.

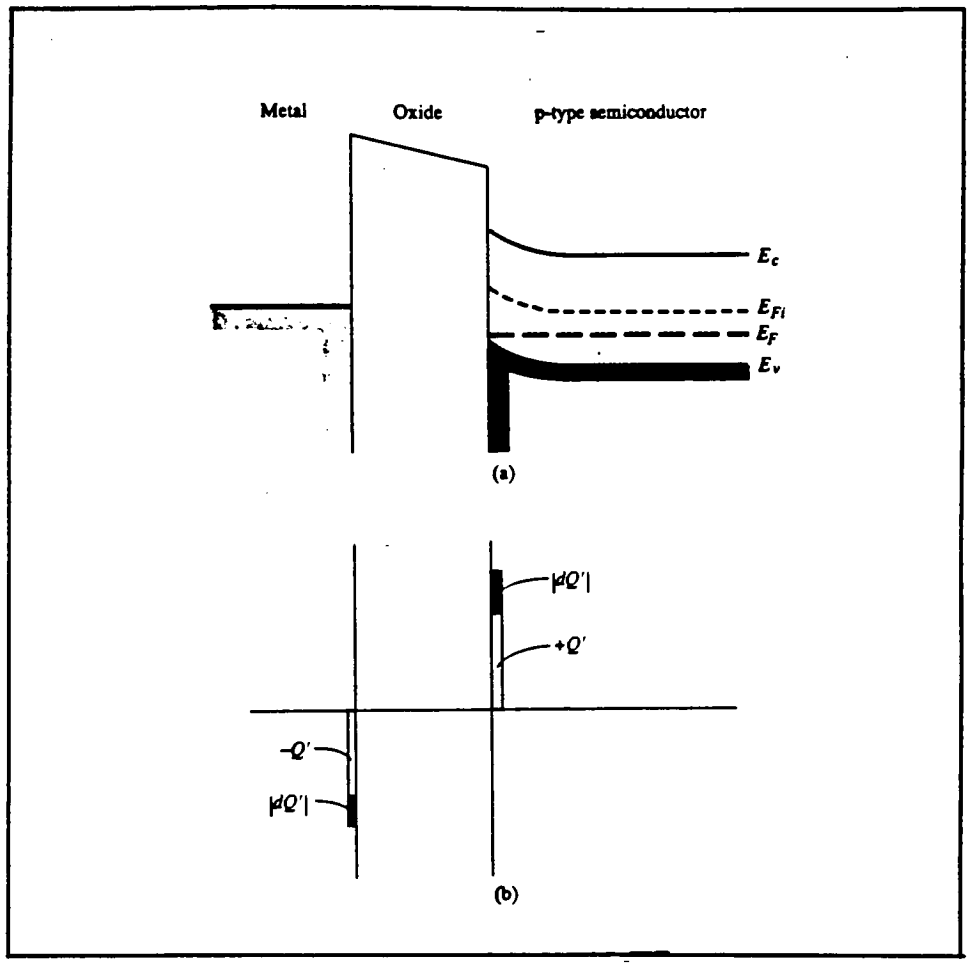


Fig. 1.6.1. (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage from reference [10]

There are three operating conditions of interest in the MOS capacitor: accumulation, depletion, and inversion. In the case of accumulation, Fig. 1.6.1a. shows the energy-band diagram of a MOS capacitor with a p-type substrate for the case when a negative voltage is applied to the gate, creating an accumulation layer of holes in the semiconductor at the oxide-semiconductor interface. A small differential change in voltage

across the MOS structure will case a differential change in charge on the metal gate and also in the hole accumulation charge, as shown in Fig..1.6.1b. The differential changes in charge density occur at the edges of the oxide, as in a parallel-plate capacitor. The capacitance C' per unit area of the MOS capacitor for this accumulation mode is just the oxide capacitance, or

$$C' (acc) = C_{ox} = \varepsilon_{ox}/t_{ox} \qquad (1.6.1)$$

In the case of depletion, Fig. 1.6.2a. shows the energy-band diagram of the MOS device when a small positive voltage is applied to the gate, creating a space charge region in the semiconductor. Fig. 1.6.2b. shows the charge distribution through the device for this condition. The oxide capacitance and the capacitance of the depletion region are in series. A small differential change in voltage across the capacitor will cause a differential change in the space charge width. The corresponding differential change in charge densities are shown in this figure. The total capacitance of the series combination is less than the oxide capacitance. As the space charge width increases with the increase of applied voltage, the total capacitance in the depletion case decreases. In the condition of the threshold inversion point, the maximum depletion width is reached but there is essentially zero inversion charge density. This condition will yield a minimum C_{min} of total capacitance.

Fig. 1.6.3a. shows the energy-band diagram of this MOS device for the inversion condition. In the ideal case, a small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density. The space charge width does not change. In the inversion, charge can respond to the change in the

capacitor voltage as indicated in Fig. 1.6.3b. then the capacitance is again just the oxide capacitance, or

$$C' (inv) = C_{ox} = \varepsilon_{ox}/t_{ox} \qquad (1.6.2)$$

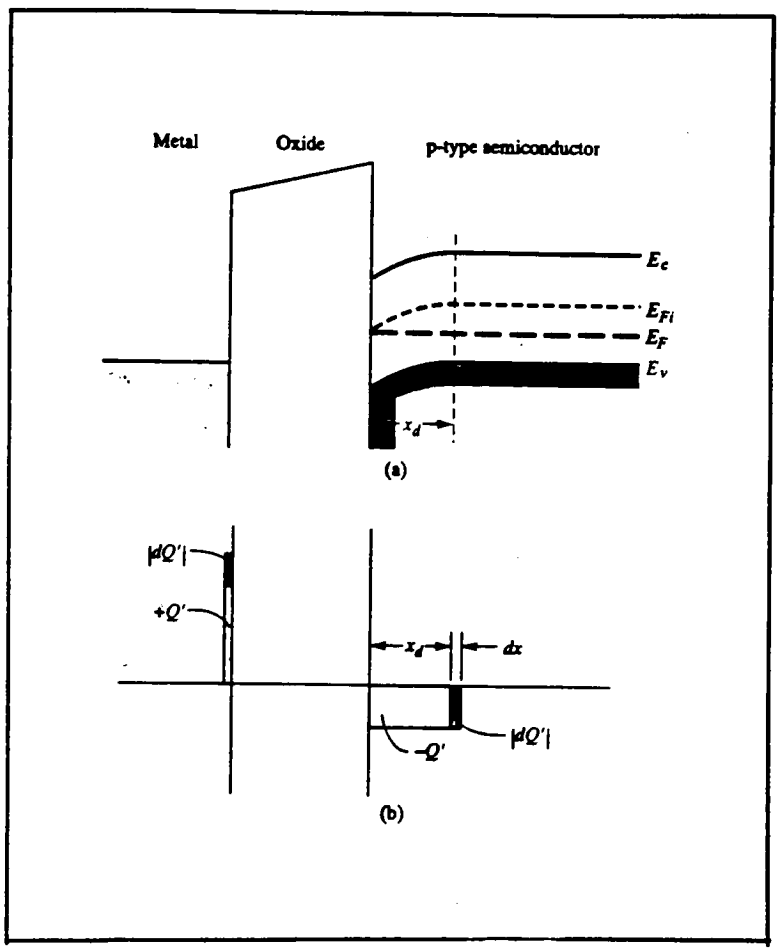


Fig. 1.6.2. (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage from reference [10]

The MOS capacitor with a p-type substrate and biased in the inversion condition is shown in Fig. 1.6.3a. We have argued that a differential change in the capacitor voltage in the ideal case causes a differential change in the inversion layer charge density. However,

we must consider the source of electrons that produces a change in the inversion charge density. There are two sources of electrons that can change the charge density of the inversion layer. The first source is by diffusion of minority carrier electrons from the p-type substrate across the space charge region. This diffusion process is the same as that in a reverse-biased pn junction which generates the ideal reverse saturation current. The second source of electrons is by thermal generation of electron-hole pairs within the space charge region. This process is again the same as that in a reverse-biased pn junction which generates the reverse-biased generation current. Both of these processes generate electrons at a particular rate. The electron concentration in the invasion layer, then, cannot change instantaneously. If the ac voltage across the MOS capacitor changes rapidly, the change in the inversion layer charge will not be able to respond. The C-V characteristics will then be function of the frequency of the ac signal used to measure the capacitance.

The high-frequency and low-frequency limits of the C-V characteristics are shown in Fig. 1.6.4. In the limit of a very high frequency, the inversion layer charge will not respond to a differential change in capacitor voltage. The capacitance of the MOS capacitor is then C_{min}. In general, high frequency corresponds to value on the order of 1 MHz and low frequency corresponds to the values in the range of 5 to 100 Hz. Typically, the high-frequency characteristics of the MOS capacitor are measured.

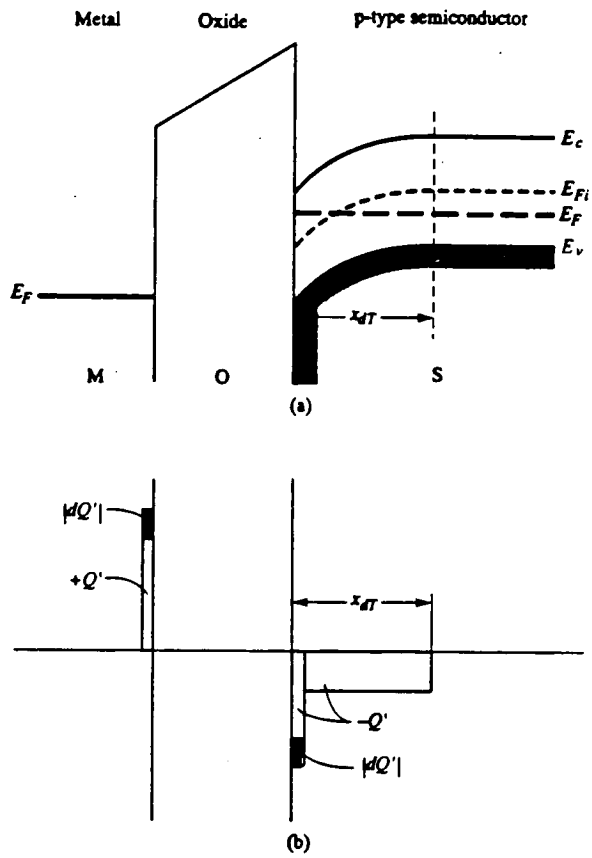


Fig. 1.6.3. (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a differential change in gate voltage from reference [10]

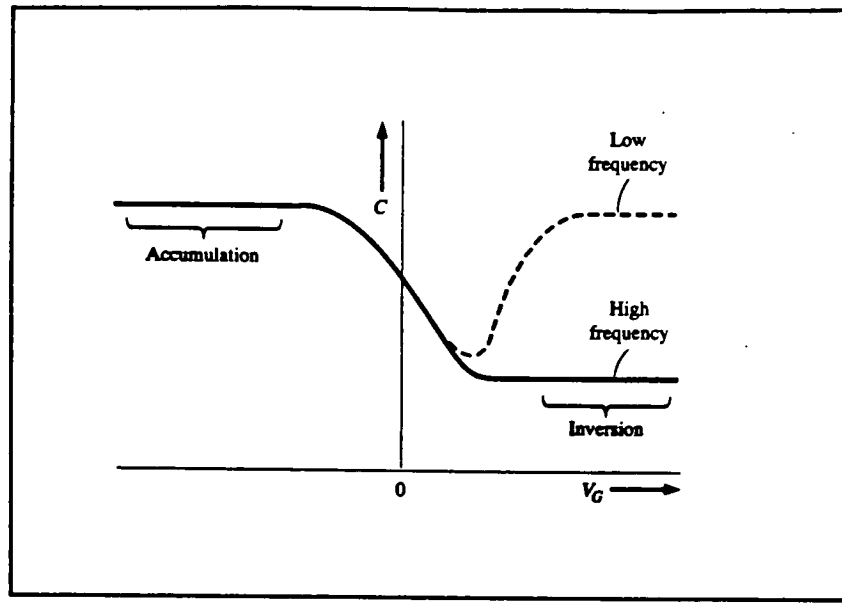


Fig. 1.6.4. Low-frequency and high-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate. From ref.[10]

1.6b. DRAM's Storage Charge Capacitor[11]

The concept of the DRAM was patented by Dennard of IBM in 1969, and the first commercial DRAM was introduced by Intel in 1970. Dynamic random access memories (DRAM's) are so named because their cells can retain information only temporarily (on the order of milliseconds); even with power continuously applied. The cells must therefore be read and refreshed at periodic intervals. The earliest DRAMs used three-transistor cells and were fabricated using PMOS technology. However, DRAM cells consisting of only one transistor and one capacitor were quickly implemented, and such cells have been used in DRAMs ever since. In order to pack a great many cells onto a DRAM chip, the cell size is made as small as possible. This implies that it is also desirable to make the area of the

storage charge capacitor as small as possible. On the other hand, Q_s of the storage capacitor must be large enough to send a sufficiently strong signal to the sense circuit.

The DRAM cell with one-transistor and one-capacitor is shown in Fig.1.6.5. The significance of this one-transistor cell is considered to be comparable to that of the invention of the transistor itself. The design of this cell has been rendered in many versions since its invention. The first such cell was fabricated with 8-μm features, used 1280-μm^2 of silicon area, and was employed in the design of the 4-kbit NMOS DRAM.

It is clear that the cell's storage capacity could be increased by making the capacitor dielectric thinner, by using an insulator with a larger dielectric constant, or by increasing the area of the capacitor. However, capacitor dielectrics thinner than that of SiO_2 now being used in DRAM cells (11 nm) will suffer leakage due to Fowler-Nordheim tunneling. Since the 256-kbit DRAM generation, a bilayer films consisting of both silicon nitride and SiO_2 have been used as the capacitor dielectric to increase cell capacitance as shown in Fig. 1.6.6. The higher dielectric constant of Si_3N_4, twice as large as that of SiO_2, was responsible for the increase.

Trench-capacitor structures have been developed as a way to achieve DRAM cells with larger capacitance values without increasing the area these cells occupy on the chip surface. The earliest one was reported in 1982 as shown in Fig. 1.6.7. The processing technology that made these structures possible was anisotropic etching of Si by RIE. Earlier V-groove structures etched in Si by means of wet etching resulted in crystallographically produced sharp edges, which in turn degraded the gate-oxide integrity. One of the first requirement test that had to be met by RIE-etched trench

capacitors was that of exhibiting breakdown characteristics equal to those of planar-type capacitors.

Another approach that allows the cell to shrink in size without a loss of storage capacity is that of stacking the storage capacitor on top of the access transistor, as shown in Fig. 1.6.8. The lower electrode of the stacked capacitor is in contact with the drain of the access transistor, and the bit line runs over the top of the stacked capacitor. For stacked capacitor cell to be made feasible for 1-Mbit DRAMs and beyond, an insulator with a larger dielectric constant than that of SiO_2 must be used, or novel cell structures must be developed. Currently, the only acceptable insulator with a sufficiently higher dielectric constant is tantalum pentoxide.

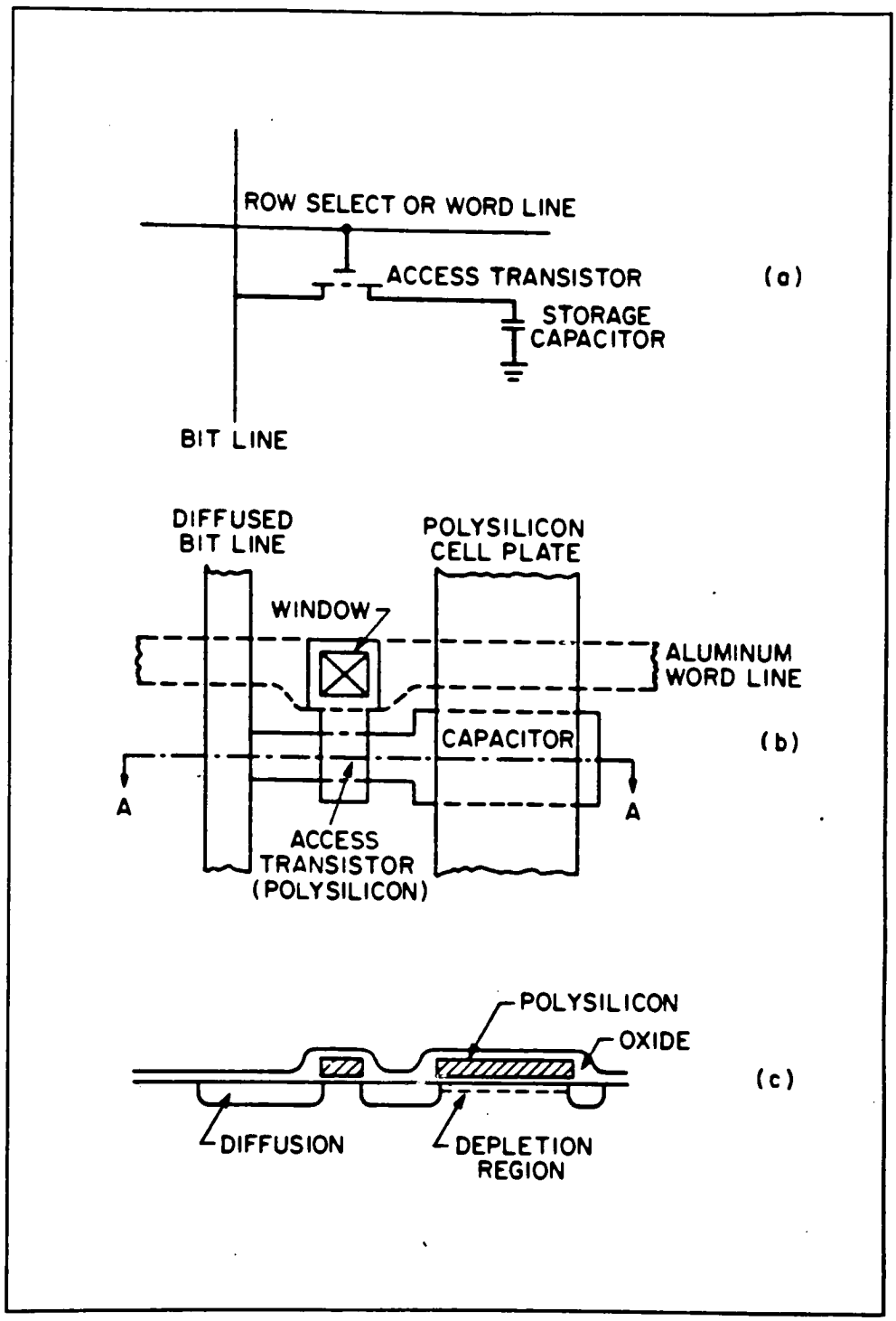


Fig. 1.6.5. DRAM cell with one transistor and one storage capacitor.
(a) Circuit schematic. (b) Cell Layout. (c) Cross section from reference [11]

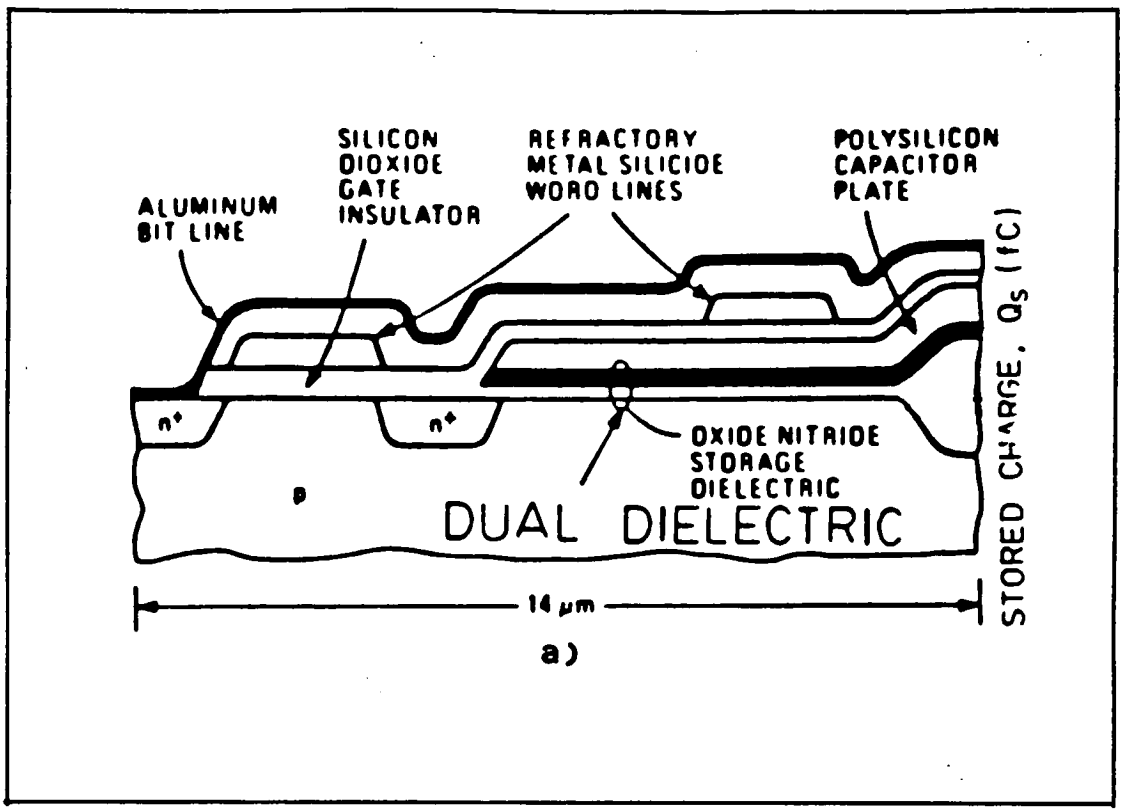


Fig. 1.6.6. Cross-sectional view of a planar capacitor DRAM cell with a two-layer capacitor dielectric from reference [11]

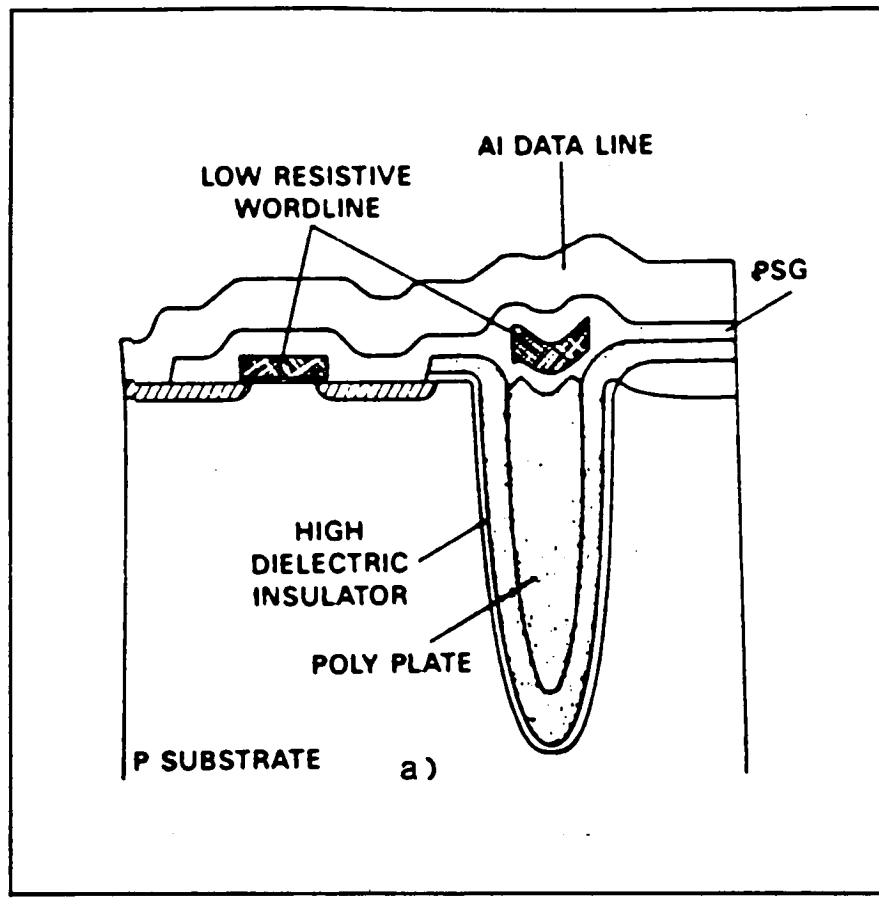


Fig. 1.6.7. Basic DRAM trench capacitor structure from reference [11]

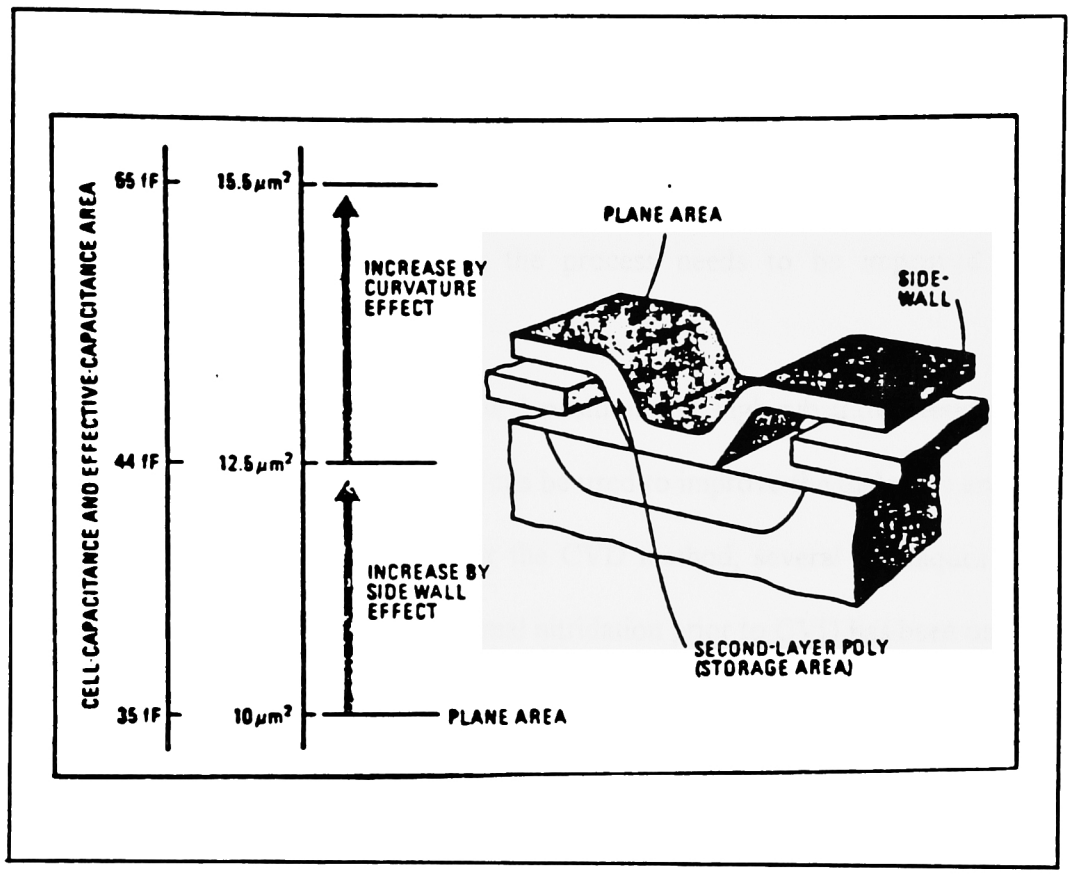


Fig. 1.6.8. Stacked capacitor cell structure from reference [11]

1.7. Deposition Processes for Tantalum Oxide Thin Films (A Review)

Two techniques, sputter deposition and CVD, have been used to make tantalum oxide films in the IC industry. In order to obtain the require of device characteristics designed, the related properties, such as breakdown voltage, leakage current, and step coverage, have to been studied. So the process needs to be improved and some subsequent processes may be required.

For the sputtering technique, low deposition rate, high substrate temperature and subsequent high temperature annealing can be used to improve the dielectric and electrical properties of tantalum oxide films. For the CVD method, several techniques have been used. One technique is that a rapid thermal nitridation prior to CVD has been used to build a layer between the tantalum oxide and the silicon substrate in order to prevent the diffusion of oxygen into the silicon to avoid growing a silicon oxide layer. Other one is that an ultraviolet irradiation has been introduced during CVD in order to improve the growth of a defect-free tantalum oxide film. The last one is that an ozone atmosphere annealing or ozone annealing with ultraviolet irradiation has been developed.

1.7a. Sputtering Deposition Process

As earlier as 1962, Silcox and Maissel studied the sputtered tantalum film capacitor and reported some factors controlling gross leakage current [12]. In 1969, Axelrod and Schwartz reported the interstitial and substitutional impurity effects and direct detection on flaw breakdown in tantalum/Ta_2O_5/metal structure [13]. In 1982,

Ohta's group reported the stacked high-capacitance RAM using tantalum oxide film for high density VLSI RAM [14]. Also in this year, Elta's group reported the tantalum oxide capacitors for GaAs monolithic integrated circuits [15]. In 1988 and 1990, Dr. Tzeng's group at Auburn University reported the high-performance tantalum oxide capacitors [16,17]. They sputtered the tantalum oxide film as thickness of 120 nm with capacitor structure of $Al/Ta_2O_5/Ta/SiO/Si$ and studied leakage current, breakdown voltage and time to breakdown.

In 1986 a research group at Hitachi Ltd. reported the leakage current increase in amorphous Ta_2O_5 films due to pinhole growth during annealing below 600°C [18]. In 1987 they reported the ultra-thin Ta_2O_5 dielectric film for high-speed bipolar memories [19]. In 1989, they also reported oxidized Ta_2O_5/Si_3N_4 dielectric films on poly-crystalline Si for DRAM's [20]. In 1990, they reported promising storage capacitor structures with Ta_2O_5 thin film for low-power high-density DRAM's [21].

To scale down VLSI's, it is necessary to reduce the device size. However, conventional films, such as Si_3N_4/SiO_2 on polycrystalline silicon have reached their physical limits in terms of thinning . This is because the direct tunnel current greatly increases below an effective SiO_2 film thickness of 5 nm. In order to ensure the required capacitor for low-power beyond 4Mb, three kinds of capacitors are proposed: SIS, MIS, and MIM. The results have revealed that the SIS, MIS, and MIM structures that have equivalent SiO_2 thickness of 5, 4, and 3 nm, respectively, can be applied to 3.3 V operated 16-Mb DRAM's and the MIS and MIM structures having equivalent SiO_2 thickness of 3 and 1.5 nm, respectively, can be applied to 1.5 V operated 64-Mb DRAM's.

A film of Ta_2O_5 was deposited by rf sputtering from a Ta target (99.99% purity) using an Ar/O_2 mixture as the sputtering gas. The total pressure of gas mixture with 10% O_2 was held at 5 mTorr. The rf power was held at 300 W. The deposition rate was 0.1 nm/min. The four configurations of plane capacitors fabricated on n-type wafers are:

a) polysilicon/ Ta_2O_5/SiO_2/polysilicon

b) polysilicon/SiO_2/ Ta_2O_5/SiO_2/polysilicon (SIS)

c) tungsten/ Ta_2O_5/SiO_2/polysilicon (MIS)

d) tungsten/ Ta_2O_5/polysilicon (MIM)

The thermal stability of films between Ta_2O_5 and electrodes was measured at 600°C, 800°C and 1000°C, respectively, for 30 min in a nitrogen atmosphere. Figure 1.7.1. shows the dependence of applied voltage required to induce a leakage current of 10^{-8} A/cm^2 on the capacitors as structures SIS, MIS and MIM. Figure 1.7.2. shows the dependence of effective field at leakage current of 10^{-6} A/cm^2 on annealing temperature.

Many stages of IC processing are carried out at high temperatures so that to understand the effect of annealing conditions on the tantalum oxide film is necessary. In 1992, Park and Baek in Korea reported the effects of annealing conditions on the properties of sputtered and LPCVD deposited Ta_2O_5 thin film [22].

The samples were prepared by dc magnetron sputtering with tantalum target of 99.9% purity. Subsequently, the tantalum films were oxidized for 1 hr. in dry O_2 at 500°C in standard oxidation furnace. The Ta_2O_5 films were annealed at temperature ranging of 700 to 950°C in dry O_2 for 20 min. The thickness was measured using an ellipsometer to be 19 nm and 35 nm.

The refractive index of 19 nm thick Ta_2O_5 film as a function of annealing temperature is shown in Fig.1.7.3. Refractive index increases sharply at 750°C and then stays about constant values with further increase in annealing temperature. It is considered to be related to the crystallization of amorphous Ta_2O_5 film during annealing.

The capacitor was structured as metal/oxide/p-Si to study electrical and dielectric properties. The I-V characteristics of 19 nm Ta_2O_5 film annealed at various temperatures in oxygen or nitrogen atmosphere shows that the leakage current decreases with temperature increase from 700 to 900°C. The C-V curves of annealed samples are negatively shifted comparing with as-oxidized sample. It suggests that the decrease in negative charge residing in Ta_2O_5 film is caused not only by the reduction of oxygen deficiency in Ta_2O_5 but also by microstructure change due to crystallization or short range order of amorphous. The dielectric constant of Ta_2O_5 films were calculated from the results of accumulation capacitance at 1 MHz as shown in Fig. 1.7.4. The effective dielectric constant of 19 nm film annealed at 750°C is slightly larger than those of the as-oxidized film and the film annealed at 700°C. This suggests that the crystalline film has larger dielectric constant than amorphous film. However, the dielectric constant decreases with increase annealing temperature above 800°C. This could be explained in terms of the growth of a SiO_2 layer at Ta_2O_5/Si interface.

In 1993 a research group at the Rensselaer Polytechnic Institute reported the tantalum suboxide film sputtered at low temperature and low rate without further annealing [23]. The advantage of this technique is that the Ta_2O_5 film can be sputtered on a such substrate, for example, glasses, which cannot stand high temperature processing.

The experiment was carried out by a dc sputter with sputtering voltage 1000V and current of 50 to 60 mA under the pressure 23 mTorr of Ar/O_2 mixture flow. The sputtering power density was 1 W/cm^2. The target temperature ranged from 190 to 200°C and the substrate temperature was 10°C lower than the target. The growth rate was 0.15 um/hr which was much lower than the conventional sputtering rate. At 190°C substrate temperature and without further annealing, tantalum suboxide film with a dielectric constant of 21-22 and a leakage current density as low as 10 nA/cm^2 at 0.5 MV/cm electrical field strength (5V of applied voltage) is obtained.

In 1994 Fujikawa and Taga at Toyota Central Research and Development Lab. Inc. reported the effects of sputtering temperature with various oxygen fractions and additive elements on Ta_2O_5 film [24]. They found that the high oxygen fraction, the high substrate temperature and the additive elements of W and Y could improve the refractive index and breakdown field strength of tantalum oxide film without further annealing.

An rf sputtering apparatus was used with a Ta_2O_5 ceramic target and pressure at 5.0 mTorr. The Ta_2O_5 film was formed under various discharge powers, 100, 300 and 500 W, and various O_2 fractions, 10%, 30% and 50%, in the total gas (Ar/O_2) amount. The substrate temperature was maintained at room temperature or 300°C. The results of refractive index and breakdown field strength are shown in Figs. 1.7.5. and 1.7.6.

Another oxide such as Al_2O_3, SiO_2, GeO_2, ZrO_2, BiO_2, Nb_2O_5, Y_2O_3 and WO_3 was added by simultaneously cosputtering into the Ta_2O_5 matrix at a temperature of 300°C for further improvement of its dielectric properties. The concentrations of additives in the films was quantitatively analyzed by Rutherford backscattering spectroscopy (RBS). The

results reveals that W, Y and Nb are good additives for both properties, i.e. high breakdown strength and large dielectric constant.

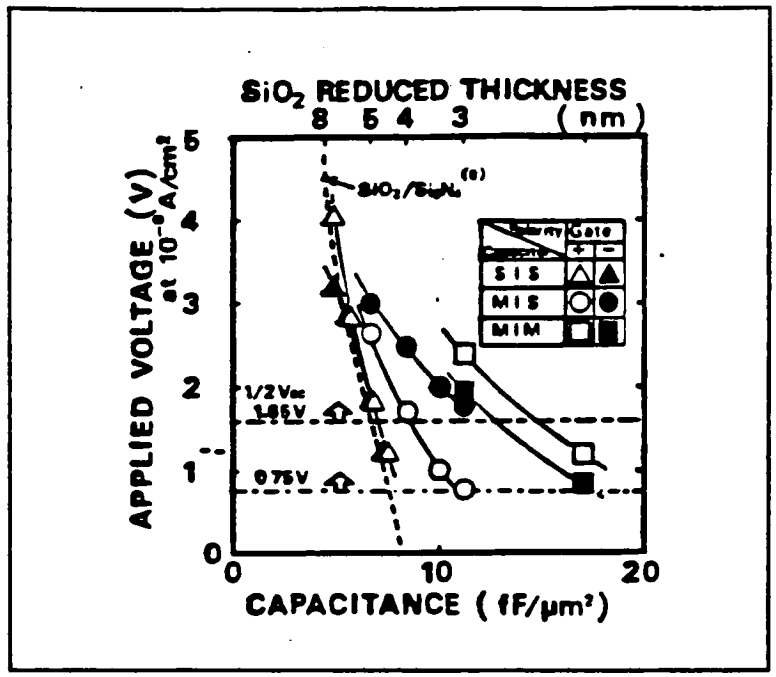


Fig. 1.7.1. Dependence of capacitance on applied voltage in Ta_2O_5 capacitors at leakage current of 10^{-8} A/cm^2 from reference [21]

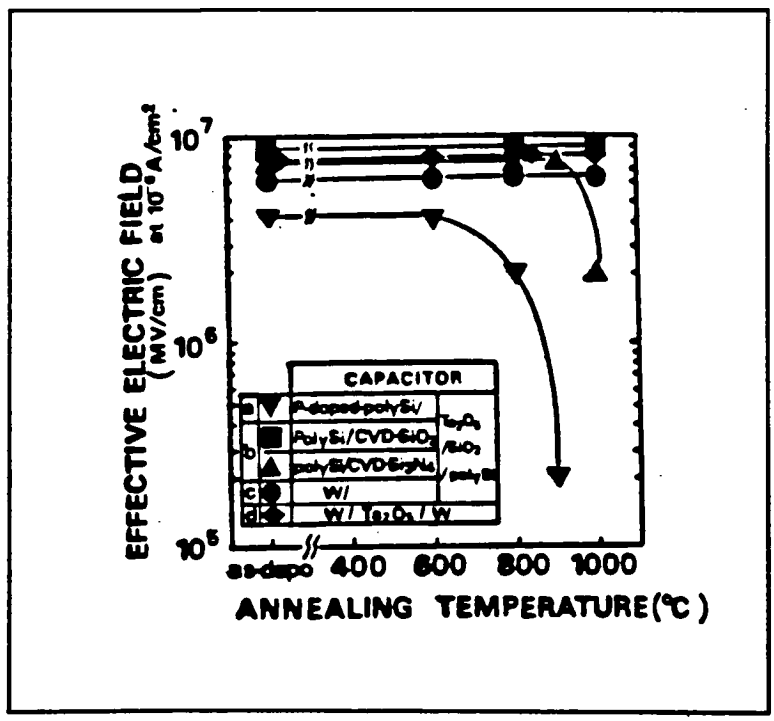


Fig. 1.7.2. Dependence of effective field on annealing temperature in Ta_2O_5 capacitors at leakage current of 10^{-8} A/cm^2 in nitrogen ambient from reference [21]

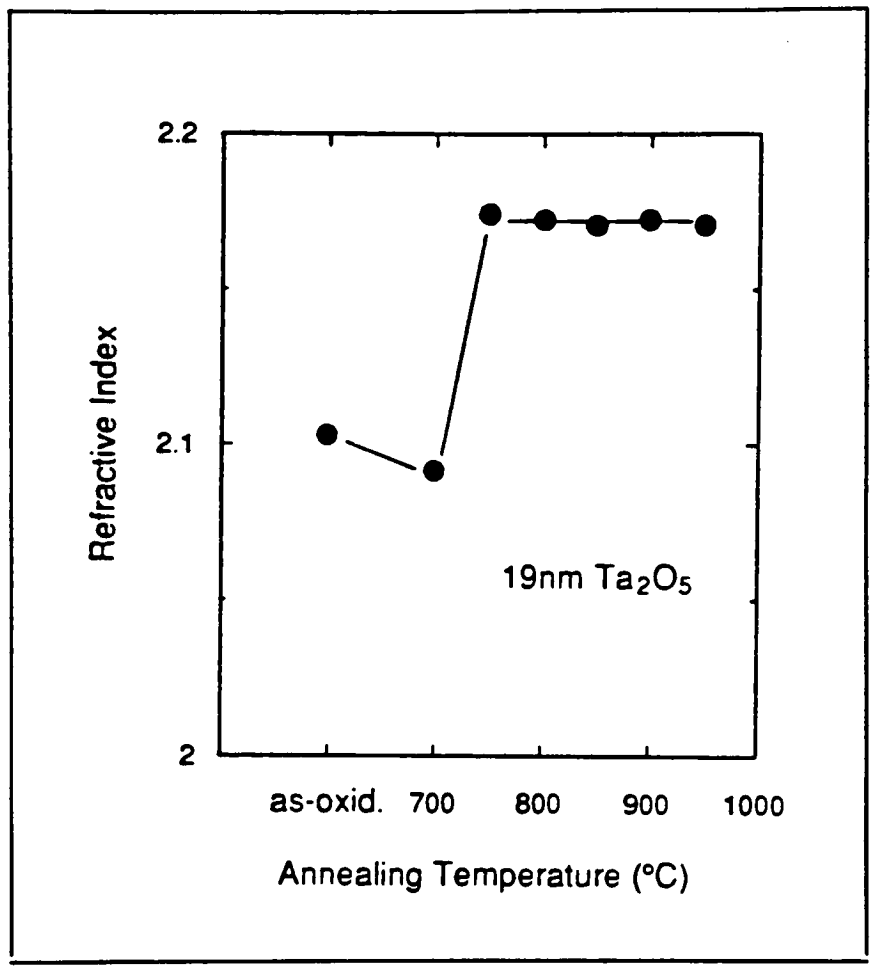


Fig. 1.7.3. Refractive index of 19 nm Ta_2O_5 vs. annealing temperature from reference [22]

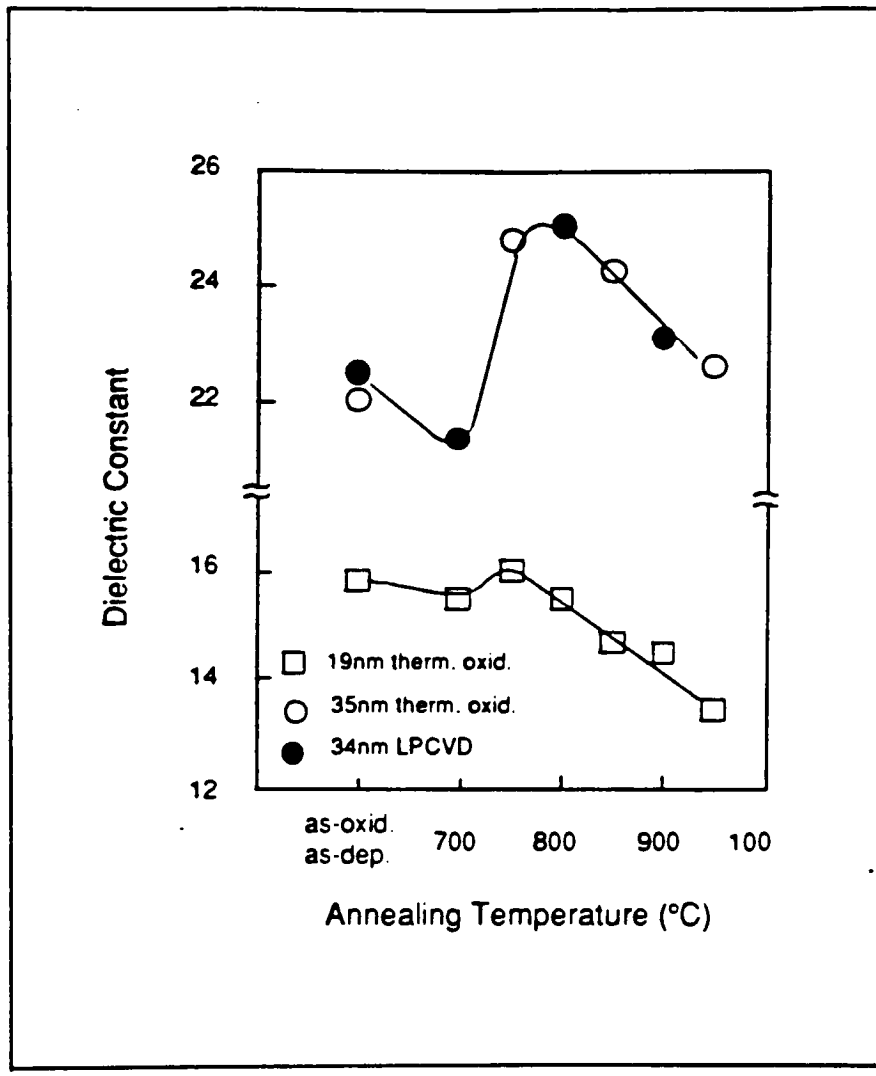


Fig. 1.7.4. Effective dielectric constant of Ta_2O_5 vs. annealing temperature. from reference [22]

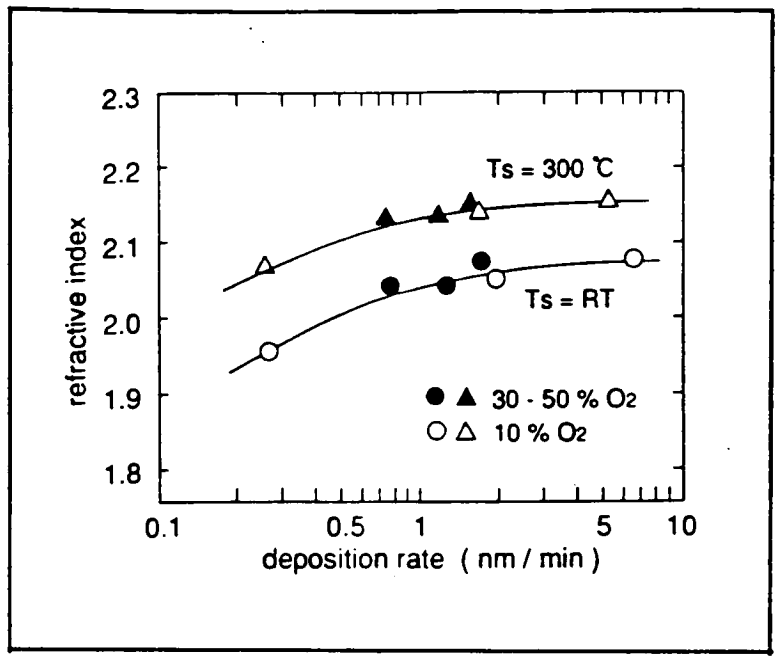


Fig.1.7.5. Dependence of refractive index of Ta_2O_5 films on deposition rate and substrate temperature from reference [23]

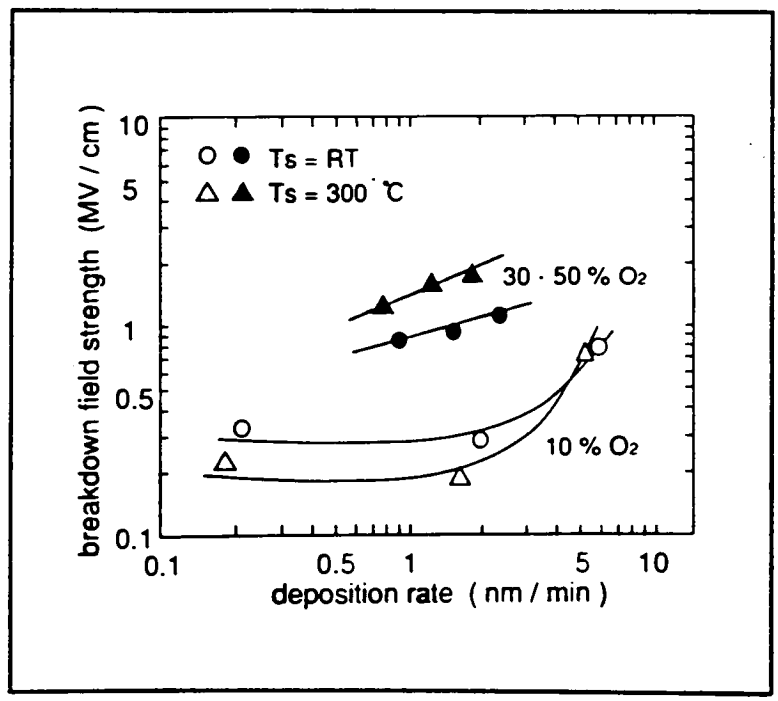


Fig. 1.7.6. Dependence of breakdown field strength of Ta_2O_5 films on deposition rate and substrate temperature from reference [23]

1.7b. CVD Deposition Process

As mentioned in section 1.7a., a research group at Hitachi Ltd. that studied the sputtered Ta_2O_5 film, were also interested in CVD processing to obtain Ta_2O_5 film . In 1989 they reported Ta_2O_5 film using CVD process [25]. In 1991 they reported UV-O_3 and dry-O_2 annealed CVD Ta_2O_5 film for storage dielectrics in 64-Mb DRAM's [26]. The reason for them to try CVD instead of sputtering was that the step coverage of sputtered Ta_2O_5 film had been found to be insufficient for application to a three-dimensional memory cell. Step coverage of CVD Ta_2O_5 film was superior to that of a sputtered film. Unfortunately, as-deposited CVD Ta_2O_5 film had a large leakage current so that additional treatment of UV-O_3 annealing was needed.

This new technique was developed to obtain extremely thin Ta_2O_5 film with an effective SiO_2 film thickness down to 2.8 nm for 1.5 V 64-Mb DRAM's. The first annealing step was ozone annealing with ultraviolet light irradiation which was the most effective on reducing leakage current. Excited oxygen atoms generated in ozone gas irradiated by mercury lamp repair the oxygen vacancies existing in the as-deposited CVD Ta_2O_5 film, resulting in a marked reduction of leakage current. The second step was dry-O_2 annealing, which reduced the defect density of initial breakdown.

In CVD process, penta-etoxy-tantalum $Ta(OC_2H_5)_5$ was evaporated and introduced to the furnace by a nitrogen carrier gas, at the same time as oxygen was introduced. The total gas pressure was kept at 80 Pa and the reaction temperature was at 420°C. After deposition, each Ta_2O_5 film was subjected to one of annealing steps. First was UV-O_3 annealing under light intensity of 100 mW/cm^2 with 185 and 254 nm

irradiation of mercury lamp. The substrate was heated to 300°C. Second was dry-O_2 annealing at temperature of 800°C. The third annealing process involved two steps, UV-O_3 annealing and following dry-O_2 annealing. The dry-O_2 annealed sputtered Ta_2O_5 film was also prepared to compare with CVD Ta_2O_5 film. The result was a leakage current of two-step treated CVD Ta_2O_5 film comparable to that of dry-O_2 annealed sputtered Ta_2O_5 film.

In 1992 a research group at Tokyo University of Agriculture and Technology reported leakage current reduction of photo-CVD Ta_2O_5 film with active oxygen annealing [27]. They optimized the substrate temperature in CVD process and the active oxygen annealing time.

Thin Ta_2O_5 films, typically with thickness of about 40 nm, were grown on n-type <100> Si wafer by UV photo-CVD using $TaCl_5$ (6N) and O_2 gas, subsequently thermal treatment. The fabrication setup was used for both CVD and active annealing steps. During photo-CVD, intense emission lines of 185 and 254 nm wavelength with intensities of 2.15 and 63 mW/cm^2, respectively, irradiated onto substrate surface. The substrate temperature was at 400 C and the deposition rate was about 1.0 nm/min. After CVD, one of the following annealing steps, O_2 ,UV-O_2, O_3, UV-O_3 , N_2 and UV-N_2, was performed on the deposited Ta_2O_5 film at temperature of 400°C and pressure of 1 atm.

Figure 1.7.7. shows refractive index and relative dielectric constant for Ta_2O_5 film deposited at various temperatures. Both the refractive index and the relative dielectric constant almost saturated at temperatures over 300°C. In general, increasing values of refractive index and dielectric constant means increasing film density, as a result reducing

leakage current. They also found out that the deposition rate of LPCVD and photo-CVD was dependent on temperature as shown in Fig. 1.7.8. The higher the temperature, the higher the deposition rate. Conventionally, choosing deposition temperature range of 400 to 500 C may obtain benefit not only for high deposition rate, but also for good dielectric constant.

In order to investigate the efficiencies of active oxygen annealing on as-deposited Ta_2O_5 films, the treatments were carried out at 400 C with varying time of up to 180 min. The results of leakage current vs. field strength for various annealing time at low temperature, 400 C, revealed that the optimized times for O_3 and UV-O_3 were 100 and 30 min, respectively. Increasing annealing time could not help to reduce leakage current.

In 1993 a research group at Watkins-Johnson Company reported a improved LPCVD reactor to grow Ta_2O_5 film for 64-Mb DRAM's [28]. The high quality Ta_2O_5 films were deposited as amorphous with smooth surface and leakage currents of annealed samples of 10 to 40 nm thickness were less than 10^{-9} A/cm^2 at gate voltage of 1.5 V. Effective dielectric constants decreased with increase of Ta_2O_5 film thickness, and this is explained by the presence of a thin SiO_2 layer at Ta_2O_5/Si interface.

During deposition, the wafers were supported by a quartz platform in near-vertical position . This position could reduce the probability of particle deposition on the wafers. The platform was heated to give uniform wafer temperature during deposition. An across-the-substrate temperature variation was no greater than ±1.5°C. The typical standard deviation of Ta_2O_5 film thickness was less than 1.2%.

LPCVD was carried out at temperature of 450 to 470°C and pressure of 600 mTorr with deposition rate of 7.5 nm/min. After deposition, all films were annealed in dry O_2 at 800°C for 30 min in a horizontal tube furnace. These annealing conditions were chosen to optimize the desired physical and electrical properties of Ta_2O_5 film. Lower annealing temperature and shorter annealing time gave higher leakage current, while higher annealing temperatures and longer times resulted in lower dielectric constant. The results show that the leakage current decreases and the breakdown voltage increases after annealing.

In 1993 a research group at NEC Corporation reported ultra-thin Ta_2O_5 film using rapid thermal nitridation (RTN) prior to LPCVD [29]. The amorphous Ta_2O_5 films were deposited on the nitrided polysilicon surface using $Ta(OC_2H_5)_5$ and O_2 gas mixture at 470°C. The films were annealed at 600-900°C in dry O_2. The densification of as-deposited films by annealing was to the formation of highly reliable ultra-thin Ta_2O_5 capacitors. The RTN treatment allowed a reduction of the SiO_2 equivalent thickness of the capacitor dielectric layer and resulted in superior leakage and reliability characteristics. X-ray spectrum of the as-deposited and annealed Ta_2O_5 films are shown in Fig.1.7.9. In order to obtain clear spectrum, 100 nm thick CVD Ta_2O_5 films were deposited on RTN -treated silicon substrates. The as-deposited CVD Ta_2O_5 film is amorphous, and Ta_2O_5 films annealed above 700 C in dry O_2 or N_2 atmosphere are crystallized. Analysis of the X-ray spectrum represents orthorhombic structure consisting with the ASTM card. These results show that the crystallization temperature of Ta_2O_5 film is 700°C and the annealing atmosphere has no effect on Ta_2O_5 crystallization.

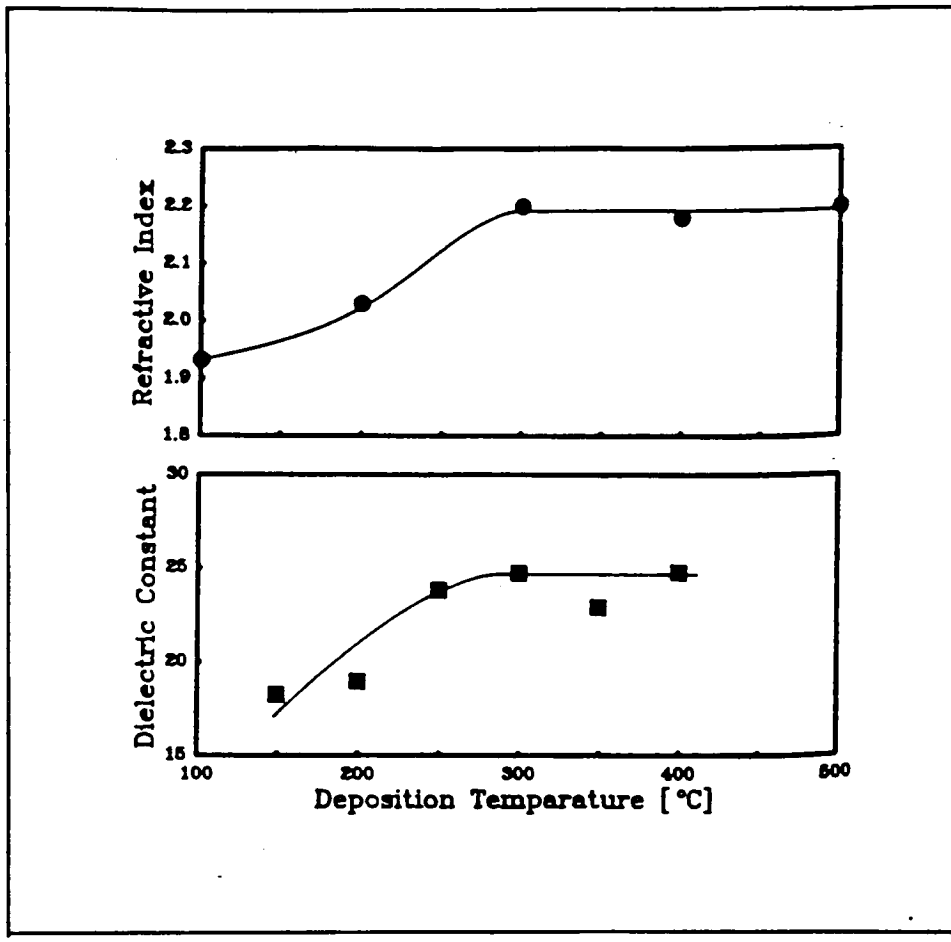


Fig. 1.7.7. Refractive index and dielectric constant of as-deposited Ta_2O_5 films vs. deposition temperature from reference [27]

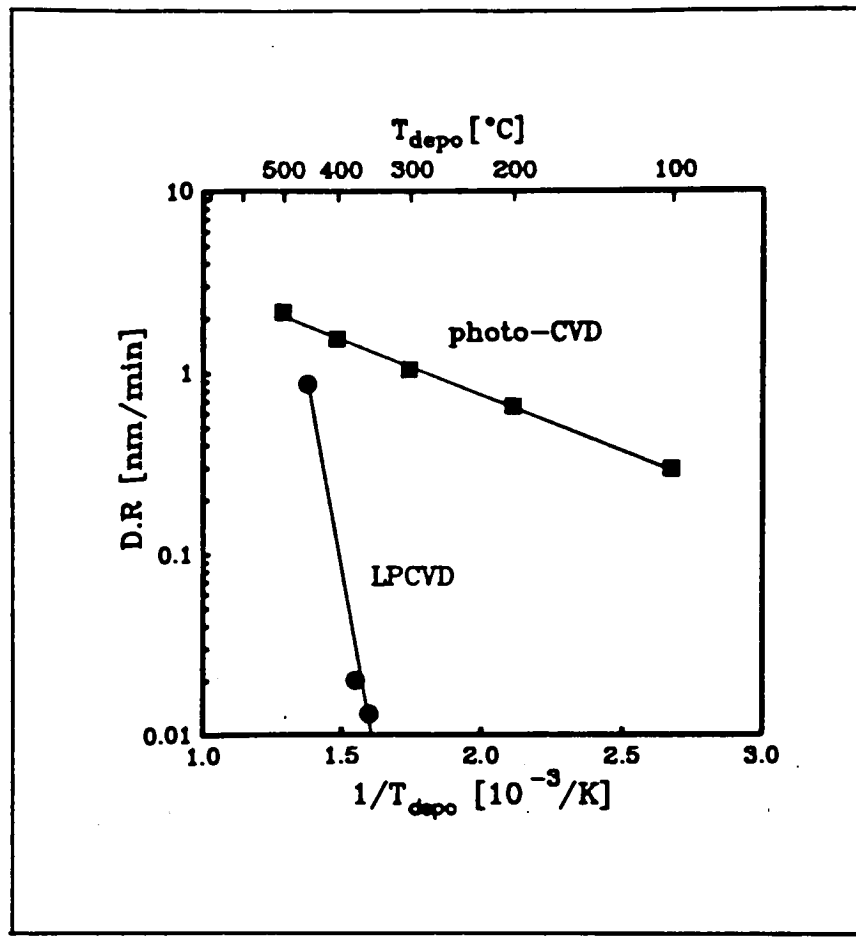


Fig.1.7.8. Correlation of deposition rate vs. deposition temperature for photo-CVD and LPCVD from reference [27]

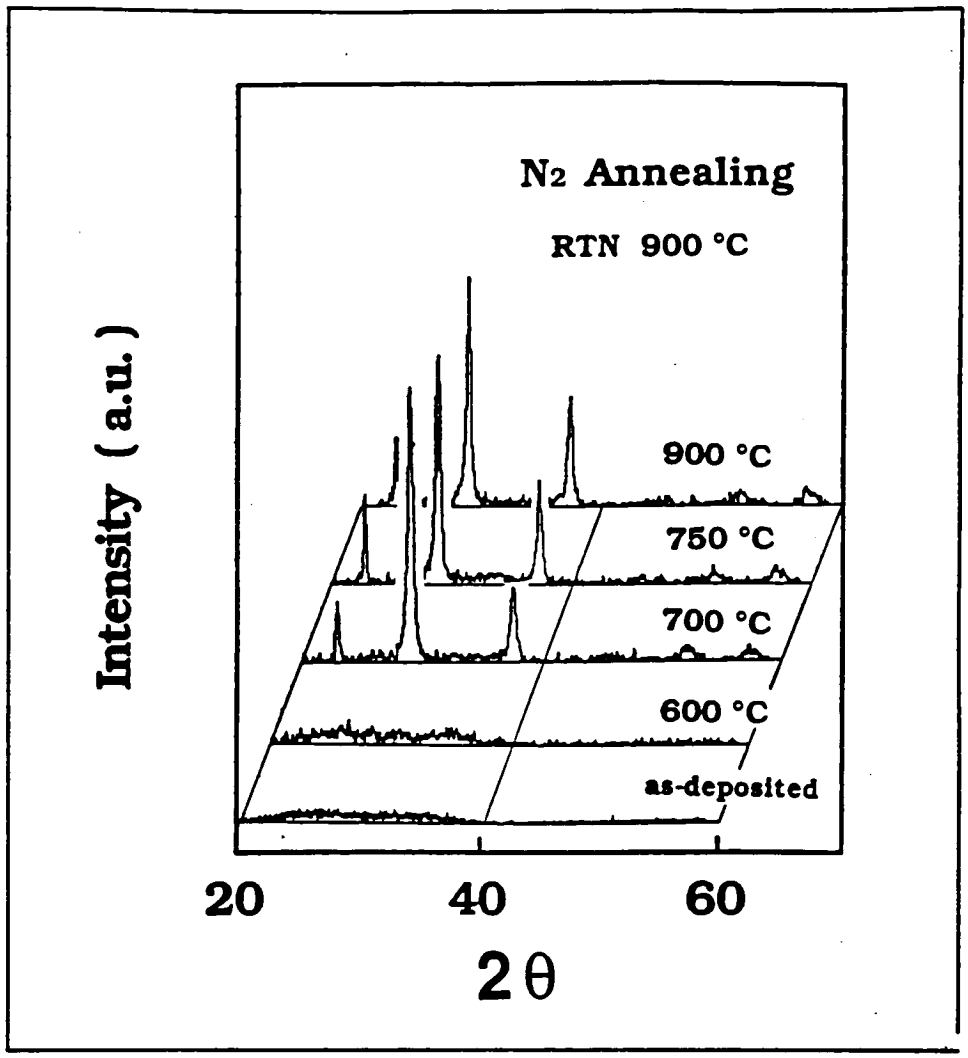


Fig. 1.7.9. Dependence of X-ray spectrum on annealing temperature in dry-N2 atmosphere. The annealing temperatures were 600-900 C. The RIN was performed at 900 C for 60 sec in NH3 from reference [29]

1.7c. Model of Leakage Current for Tantalum Oxide Thin Films

A widely accepted model for leakage current reduction by annealing is that the amorphous Ta_2O_5 films have an oxygen vacancy in the Ta-O network and it will be filled by an oxygen species after annealing. On the other hand, the interfacial SiO_2 between Ta_2O_5 and Si substrate has been reported to significantly affect the leakage current. So the way for scientists to reduce leakage current in Ta_2O_5 films is focus on reducing the number of oxygen vacancies and to suppers the SiO_2 growth during process.

1.8. Etching Process for Tantalum Oxide Thin Films (A Review)

1.8a. Wet Etch of Ta_2O_5 and Ta

Tantalum and tantalum compounds can be etched in HF. The Ta_2O_5 does not etch as rapidly as TaN and Ta in HF and therefore acts as a protector for the substrate surface. However, it is difficult to etch tantalum compounds in HF if the substrate is silica. J. Grossman at Westinghouse Electric Corporation found a new etchant which attacks tantalum and its compounds at a rate equal to, if not faster, than the etches containing HF [30] . It also attacks silica but at much slower rate than the etches containing HF.

The etchant is made up of a very highly concentrated solution of 30% sodium (or potassium) hydroxide and 30-35% hydrogen peroxide. The proportion is about 9 or 10 to 1 of NaOH to H_2O_2. A small Pyrex breaker (~50 ml) is filled half full of the NaOH solution. The solution is heated to 90 C and the H_2O_2 is added. The etch rate for Tantalum and tantalum compounds is 100-200 nm/min.

1.8b. Dry Etch of Ta_2O_5 and Ta in CF_4

There is only one reference paper dealing with reactive ion etching of sputter deposited tantalum oxide and its etch selectivity to tantalum in CF_4, CF3Cl and CHF_3 published in 1992[31]. However, this paper did not discuss the selectivity of tantalum oxide to Si and SiO_2, even though this property is important for IC process.

Process parameters that affect the etch rate of Ta_2O_5, such as the power, pressure, and temperature, were investigated in a wide range of conditions. The etch rate was

decreased by replacing one F atom in CF_4 with one Cl or H atom. The same kind of relation has been observed in the RIE of tantalum nitride. It is different from that in the RIE of tantalum. The CF_4 process is more sensitive to the substrate temperature than the CHF_3 process because of the difference in the nature of surface reaction. In the CF_4 plasma, tantalum is etched faster than tantalum oxide. However, in the CHF_3 plasma, tantalum oxide is etched faster than tantalum and the selectivity increases with the decrease of the power.

Before the etch, the film composition was uniform, and it contained tantalum in metallic and various oxidation states. After etch, the film surface contained Ta_2O_5 state only. Tantalum oxide etch mechanisms in CF_4 and CHF_3 plasmas are different. Compared with the CF_4 etched surface, the CHF_3 etched surface contained a high fluorinated organic layer that prevented the fluoride formation and that required a higher ion bombardment energy to remove.

1.8c. Dry Etch of Ta in SF_6

There is only one paper that studied plasma etching of the tantalum in SF_6 and SF_6-O_2 published in 1985 [32]. The etching rates and reaction products of refractory metals (W, Mo, and Ta) and silicon were studied in a SF_6-O_2 r.f. plasma. The highest etching rate of tantalum was found as 1 μm/min in SF_6-O_2 with a ratio of 8 to 2 at a pressure of 200 mTorr, a power of 50 W, and a flow rate of 40 sccm. The etching rate decreased with increase of oxygen. During the plasma etching of tantalum, traces of TaF_4+ and TaF_3+ were detected, but no indication of TaOFn+ was found.

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Chapter 2. Deposition Properties of Tantalum Oxide Thin Films

2.1. Experimental

2.1a. Reactive Sputter Deposition

A reactive sputter system, model CVC-601, was used to deposit Ta_2O_5 films and Ta films. The target was an 8" diameter pure tantalum. For the Ta_2O_5 film deposition, the pressure was 5 mTorr in Ar with 20% oxygen, the flow rates of Ar and O_2 were 200 and 50 sccm, respectively, and the powers were 400 W and 700 W to generate the deposition rate of 1 and 2.5 nm/min, respectively. For the Ta film deposition, the pressure was 4.5 mTorr in Ar, the flow rate of Ar was 240 sccm, and the power was 2640 W with deposition rate of 27 nm/min. The deposition of Ta_2O_5 and Ta films was at room temperature.

2.1b. Annealing

As-deposited Ta_2O_5 films were amorphous phase and their characteristics, such as dielectric constant, leakage current and breakdown voltage, were not good enough to be used as a dielectric layer in a storage capacitor so that an annealing process had to be carried out to improve the deposited films. A thermal furnace was used to anneal as-deposited films in oxygen ambient at either high or low temperatures for 30 min. The high temperature was 750 or 800°C for recrystallization. The low temperature was 450 or

600°C. The reason to choose the temperature of 750 or 800°C for recrystallization is that first, the recrystallization temperature of amorphous phase Ta_2O_5 is approximately 650°C so that the annealing temperature should be higher than this temperature, second, if the annealing temperature is very high, for example, 900 or 1000°C, the growth of SiO_2 in the interface of Ta_2O_5/Si during Ta_2O_5 annealing will be significant and the apparent dielectric constant of Ta_2O_5 film will decrease because the dielectric constant of SiO_2 is much low and the apparent constant is the combination of Ta_2O_5 and SiO_2.

2.1c. Characteristics

An ellipsometer in the wavelength of 562 nm was used to characterize the refractive index and thickness of Ta_2O_5 films as-deposited and annealed. The thickness of Ta_2O_5 film was also measured by Nanospec using the program of nitride with the index of Ta_2O_5 film itself measured by ellipsometer. The Ta_2O_5 film phase was identified using an X-ray diffractometer (Rigaku DMAX B) employing Cu K-alpha radiation.

2.2. Two-step Process of Tantalum Oxide Thin Films

A two-step process was proposed to improve the characteristics of active sputter deposited Ta_2O_5 films. The process was designed that, at the first step, the films were deposited as thickness of approximately 20 nm and annealed at temperature of 750°C to recrystalline, then, at the second step, a second layer of Ta_2O_5 film was deposited increasing the thickness up to 60 nm and annealed at temperatures of 420, 600 or 750°C. The purpose of a two-step process is to optimize annealing temperature in order to obtain

high quality of Ta_2O_5 thin films as the target of high dielectric constant and low leakage current. Typically, the leakage current contributed by vacancies will increase if the grain boundary increases or the grain columns is along the direction of applied voltage of capacitor. So the amorphous state of the Ta_2O_5 film could have less leakage current than the recrystallized film. However, the amorphous state is less condensed to promote low index and dielectric constant. The idea of two-step process wants the second layer of Ta_2O_5, which is deposited on the recrystallized first layer rather than on the silicon substrate, to be easily condensed so that the whole two-layer film will have low leakage current and high dielectric constant.

2.3. Results and Discussions

The X-ray spectrum of recrystalline Ta_2O_5 film is shown in Fig. 2.3.1. The X-ray sample with thickness 88 nm was annealed at temperature of 800°C for 30 min. The reason to use the thick film was to obtain a strong signal to identify the X-ray spectrum of Ta_2O_5 structure. The analysis of the spectrum of the recrystallized Ta_2O_5 film matches the ASMT card, No: 8-225, as orthorhombic structure.

The thickness/index variations of Ta_2O_5 films annealed at high temperature are shown in Table 2.3.1. That the films are condensed after annealing at high temperature is an evidence of recrystallized Ta_2O_5 film. The increase of refractive index can predict that the dielectric constant will increase. But the values of refractive index are still less than the value of 2.18 of CVD Ta_2O_5 films. An interesting phenomenon is that the thickness decrease, delta th in Table 2.3.1, of thin samples 1, 2, 3, and 4 is almost the same as that

of the thick samples 5 and 6 even though the relative condensations of thin samples are larger than the thick samples. It suggests that there is an layer of incompletely oxidized tantalum or sub-stoichiometric structure of Ta_2O_5 in the Si/Ta_2O_5 interface as the film was deposited. During annealing, this layer can condense more than the Ta_2O_5 film. In other words, in terms of the concept of amorphous state, there are more free volumes in this interface layer rather than in the Ta_2O_5 film so that the main part of thickness decrease was contributed from this layer.

The thickness/index variation of Ta_2O_5 films during two-step process is shown in Table 2.3.2. Sample 7 was deposited for a single layer as a control wafer in the second step to investigate the changes of thickness and refractive index of single layer comparing to double layers in the second step.

Comparing the thickness of control wafer, sample 7, with single layer to the thickness increase of samples 2, 3, and 4 with double layers in the second deposited, it is found that the thickness increase of samples 2, 3, and 4 are less than the thickness of sample 7 as shown in Table 2.3.3. It suggests that the second layer deposited on the annealed first layer is more condensed than the single layer deposited on silicon substrate. That the values of refractive index of samples 2, 3, and 4 are higher than that of sample 7 can also be explained by the more condensed second layers. It can be considered that the annealed first layer is easier for Ta_2O_5 film to grow up than silicon substrate.

Table 2.3.4. shows the thickness decrease at different temperatures. It shows that the thickness decrease of double layers is less than that of single layer. It also gives an

evidence that the second layer is more condensed during deposition so that it could not condense more in second annealing rather than single layer.

The advantage of two-step process is to obtain Ta_2O_5 films which are more condensed and have higher refractive index. The higher refractive index predicts higher dielectric constant.

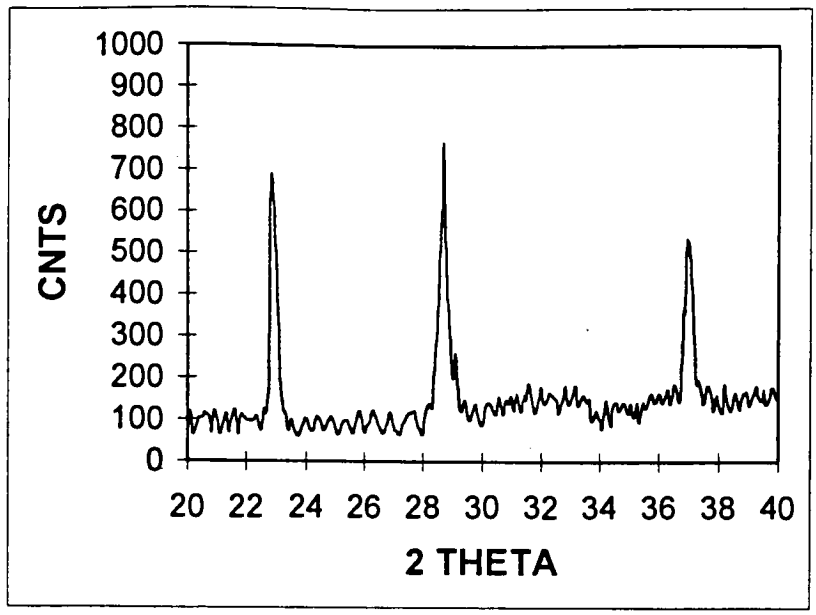


Fig. 2.3.1. X-ray diffraction spectrum of Ta_2O_5 film annealed at 800°C for 30 min in oxygen

Table 2.3.1. Variations of thickness(A)/index of Ta_2O_5 films after high temperature annealing

Sample	Deposition	Anneal at 750C	delta th	Cond %
1	222.6/1.730	191.4/2.030	31.2	16.301
2	225.2/1.734	193.3/1.947	31.9	16.503
3	224.4/1.737	194.2/1.988	30.2	15.551
4	217.0/1.789	191.8/1.971	25.2	13.139
5	833.5/2.091	794.1/2.166	39.4	4.9616
6	880.6/2.088	834.1/2.167	46.5	5.5749

1. delta th: thickness decrease of film after annealing
2. Cond %: relative condensation = delta th/ thickness after annealing

Table 2.3.2. Variations of thickness(A)/index of Ta_2O_5 films during two-step process

Sample	First Deposition	Annealing 750C	Second Deposition	Thermal 420C	Annealing 600C	750C
2	225.2/1.734	193.3/1.947	587.4/2.069	576.6/2.082		
3	224.4/1.737	194.2/1.988	589.9/2.072		586.9/2.082	
4	217.0/1.789	191.8/1/971	585.1/2.074			576.1/2.111
7			424.3/2.014	413.2/2.051	397.7/2.078	

Table 2.3.3. Thickness increase of samples 2, 3, and 4 vs. thickness of sample7 in second deposition

Sample	First Deposition	Annealing 750C	Second Deposition	Thickness Increase
2	225.2/1.734	193.3/1.947	587.4/2.069	394.1
3	224.4/1.737	194.2/1.988	589.9/2.072	395.7
4	217.0/1.789	191.8/1/971	585.1/2.074	393.3
7			424.3/2.014	424.3

Table 2.3.4. Relation of thickness decrease to annealing temperature and layer

Sample	Temp.C	thick.A	delta th	Layer
1	750	222.6	31.2	Single
2	750	225.2	31.9	Single
3	750	224.4	30.2	Single
4	750	217	25.2	Single
5	750	833.5	39.4	Single
6	750	880.6	46.5	Single
7	420	424.3	11.1	Single
7	600	424.3	26.6	Single
2a	420	587.4	10.8	Double
3a	600	589.9	3	Double
4a	750	585.1	9	Double

1. delta th: thickness decrease after annealing
2. Temp.C: annealing temperature in C
3. thick A: film thickness before annealing
4. samples 2a, 3a, and 4a: samples 2, 3, and 4 in second step with double layers.

Chapter 3. Dielectric Properties of Tantalum Oxide Thin Films

3.1. Experimental

The way to characterize the dielectric properties in the present work is well known as a MOS capacitor method. The Ta_2O_5 film was deposited as a dielectric layer in a capacitor and the dielectric constant was calculated by the capacitance, electrode area, and Ta_2O_5 film thickness measured. At the same time, the leakage current and breakdown voltage of the Ta_2O_5 film were also studied. Various capacitor configurations, such as MIM ($Al/Ta_2O_5/Al$) and MIS (Al/Ta_2O_5/p-Si, Al/Ta_2O_5/n-Si, and Al/Ta_2O_5/n+-Si), were fabricated in order to study the interface between Ta_2O_5 film and substrate. The effect of interface on the leakage current and apparent capacitance is discussed.

3.1a. Capacitor Fabrication

In the process of capacitor fabrication, the Ta_2O_5 film was deposited using reactive sputtering model in a CVC-601, and the Al electrodes were fabricated using lithography and wet etching. The two-step process discussed in Chapter 2 was also used to build up the Ta_2O_5 dielectric layer.

The base line process of MIM ($Al/Ta_2O_5/Al$) capacitor, sample 1, with as-deposited Ta_2O_5 film is as following:

1. RCA cleaning silicon wafers
2. depositing Al film of 6000A thickness on silicon substrate

using CVC-601 active sputter

3. depositing Ta_2O_5 film of 1800A thickness on the top of Al film and other bare control wafer using CVC-601 sputter,
4. depositing Al film of 6000A thickness on the Ta_2O_5 film using CVC-601 sputter
5. patterning photoresist for Al electrodes on the samples using lithography, mask: #310346 capacitor test reticle
6. wet etching Al electrodes using hot NaOH, drain and dry
7. ashing photoresist
8. measuring the thickness and refractive index of Ta_2O_5 film on the control wafer using ellipsometer
9. measuring capacitance and conductance using C-V plotter and HP4145

The base line process of MIS ($Al/Ta_2O_5/p$-Si and $Al/Ta_2O_5/n$-Si) capacitors, samples 2 and 3, with as-deposited Ta_2O_5 film is as following:

1. RCA cleaning p-type and n-type silicon wafers
2. depositing Ta_2O_5 film using CVC-601 sputter
3. depositing Al film on the Ta_2O_5 film using CVC-601 sputter
4. patterning photoresist for Al electrodes using lithography, mask: #310346 capacitor test reticle
5. wet etching Al electrodes, drain and dry
6. ashing photoresist.

7. measuring the thickness and refractive index of Ta_2O_5 film on the control wafer using ellipsometer

8. measuring capacitance, conductance, leakage current and breakdown voltage using C-V plotter and HP4145

For the MIS ($Al/Ta_2O_5/n+$-Si) capacitor, an n+-type silicon substrate was needed. The base line for the n+-type silicon is as following:

1. 4-point test on n-type wafer

2. RCA cleaning n-type wafers

3. spinning phosphors chemical, P-8545, on silicon substrate, 3000 rpm and 30 sec

4. pushing at 900°C, N_2 5 Lpm, into furnace

5. soaking at 900°C, N_2 5 Lpm, for 15 min as phosphors pre-deposition

6. BOE etching glass for 3 min

7. phosphors drive-in in dry O_2

   a. push-in at 900°C in dry O_2, flow rate 5 Lpm

   b. ramp up to 1100°C in dry O_2

   c. soaking at 1100°C in dry O_2 for 30 min

   d. ramp down to 1000°C in dry O_2

8. BOE etching glass for 1 min, drain and dry

9. 4-point test on n+-type wafers to check the decrease of sheet resistance

The base line process of MIS ($Al/Ta_2O_5/p$-Si, $Al/Ta_2O_5/n$-Si, and $Al/Ta_2O_5/n+$-Si) capacitors, samples 4, 5, and 6, with two-step processed Ta_2O_5 films is as following:

1. RCA cleaning p-type, n-type and n+-type wafers

2. depositing first layer of Ta_2O_5 film

3. measuring thickness and refractive index of Ta_2O_5 films using ellipsometer

4. furnace annealing Ta_2O_5 films at 750°C in dry O_2 for 30 min

5. measuring thickness and refractive index of Ta_2O_5 films using ellipsometer

6. second depositing Ta_2O_5 films

7. measuring thickness and refractive index of Ta_2O_5 films using ellipsometer

8. furnace annealing films at 420, 600, or 750°C in dry O_2 for 30 min

9. measuring thickness and refractive index of Ta_2O_5 films using ellipsometer

10. depositing Al film on the Ta_2O_5 film using CVC-601 sputter

11. patterning photoresist for Al electrodes using lithography, masks: #310346 capacitor test reticle and #310283 M9112051R4 reticle

12. wet etching Al electrodes using hot NaOH, drain and dry

13. ashing photoresist.

14. measuring capacitance, conductance, leakage current and breakdown voltage using C-V plotter and HP4145

3.1b. Measurement Techniques

The C-V plotter at frequency 1 MHz was used to measure capacitance and conductance. For MOS capacitors with p-type, n-type, and n+-type substrate, the C-V plotter was ramped from -5V to +5V and the values of capacitance and conductance were obtained at the accumulation mode. Because of leakage current of capacitor, the capacitance measured is apparent, not a real value. Then an equivalent circuit of capacitor

was proposed to obtain the true value of capacitance concerning the leakage current contributed by a equivalent resistor[1]. The equation to correct capacitance is given as:

$$C_{co}=C_{ma}(1+((G_{ma}/(\omega *C_{ma}))^2) \qquad (3.1.1)$$

where C_{ma} is capacitance measured, C_{co} capacitance corrected, G_{ma} conductance measured, ω circular frequency.

The leakage current and breakdown voltage were measured using a model HP4145 parameter analyzer.

3.2. Results

The values of capacitance measured and the dielectric constant calculated in MIM capacitors of as-deposited Ta_2O_5 film, sample 1, vs. electrode areas before and after Al sintering are listed in Tables 3.2.1. and 3.2.2. The capacitor electrodes have two kinds of patterns, square and circle, with same areas from 2.0 to 0.4 mm square. The measurements are shown in both Tables 3.2.1 and 3.2.2. that the values of capacitances of square and circle patterns are the same. So we were regardless of the electrode patterns, neither square nor circle, in the further measurements. The sample was annealed using standard Al sintering procedure, i.e. at temperature 450°C for 20 min in N_2 instead of forming gas, and measured again for capacitance. The results show that the capacitances after Al sintering measured from C-V plotter did not change.

The values of capacitance and conductance measured and the dielectric constant calculated in MIS (Al/Ta_2O_5/p-Si and Al/Ta_2O_5/n-Si) capacitors with as-deposited Ta_2O_5 film, samples 2 and 3, vs. electrode areas are listed in Tables 3.2.3. The equation (3.1.1)

was used to correct the measured capacitance of MIS capacitors in order to obtain a correct value of dielectric constant. Without this correction, the dielectric constant would be smaller.

The values of capacitance and conductance measured and the dielectric constant calculated in MIS ($Al/Ta_2O_5/n+$-Si) capacitors with two-step process, sample 6, vs. electrode areas are listed in Tables 3.2.4. The samples 6a, 6b, 6c, and 6d correspond to different second annealing temperatures, i.e. no annealing, 420°C, 600°C and 750°C, respectively.

The values of capacitance and conductance measured and the dielectric constant calculated in MIS (Al/Ta_2O_5/p-Si and Al/Ta_2O_5/n-Si) capacitors with two-step process, samples 4 and 5, vs. electrode areas are listed in Tables 3.2.5. The samples 5a and 5b correspond to different second annealing temperatures, i.e. no annealing and 420°C, respectively.

Figures 3.2.1. and 3.2.2. show typical C-V curves for MIS capacitors, samples 2 and 3, measured by C-V plotter at 1 MHz, respectively. A flat band voltage of -0.6 V is calculated for sample 3 on n-Si with substrate doping of $7x10^{14}$ cm^{-3} from which total oxide trap density $Qit/q = 1.3x10^{11}$ cm^{-3} is estimated. Similar analysis could not be done for sample 2 on p-substrate.

Figures 3.2.3. and 3.2.4. show typical I-V curves for MIS capacitors, samples 2 and 3, measured by HP4145, respectively. The films on a p-type substrate can sustain an electric field of 3 MV/cm at a current density of 1 $\mu A/cm^2$ in the accumulation mode, which is an order higher than that observed in films on a n-type substrate. It was also

observed that the device on p-type substrate contributed higher leakage current in the depletion-inversion mode whereas the devices on the n-type substrates were found to be more leaky in the accumulation mode.

Figure 3.2.5. shows typical I-V curves for MIS capacitor, sample 6b, The difference of Figure 3.2.5. from Figures 3.2.3. and 3.2.4. is that the leakage current in the sample 6b below 1 MV/cm was less than the sensitivity of HP4145 so that the curve only represents noise and is not continuous. The breakdown voltage of two-step processed samples obtained from I-V curve was 3-7 MV/cm.

Table 3.2.1. Capacitance and dielectric constant of MIM capacitor with as-deposited Ta_2O_5 vs. electrode areas

A, mm^2	1.5	1	0.8	0.5	0.4
C(sq), pf	1200	790	640	390	310
C(ci), pf	1200	790	635	390	310
Const.	16.3	16.1	16.3	15.9	15.8

Table 3.2.2. Capacitance and dielectric constant of MIM capacitor with as-deposited Ta_2O_5 vs. electrode areas after Al sintering

A, mm^2	1.5	1	0.8	0.5	0.4
C(sq), pf	1200	790	620	385	305
C(ci), pf	1200	790	620	385	305
Const.	16.3	16.1	15.8	15.7	15.6

Table 3.2.3. Capacitance, conductance and dielectric constant of MIS (Al/Ta_2O_5/p-Si and Al/Ta_2O_5/n-Si)capacitors, samples 2 and 3, with as-deposited Ta_2O_5 vs. electrode areas

Sample	Configuration	Th (A)	Index	A,mm^2	Cma,pF	G, umho	Cco, pF	Const.
2	Al/Ta2O5/p-Si	214.5	1.7371	0.4	1400	3200	1585	9.6
3	Al/Ta2O5/n-Si	405.6	2.0205	0.8	630	3000	990	6.43
				0.5	480	1750	640	6.65
				0.4	400	1250	500	6.5

Table 3.2.4. Capacitance, conductance and dielectric constant of MIS (Al/Ta_2O_5/n+-Si) capacitor, sample 6, with two-step process vs. electrode areas

Sample	Configuration	Th (A)	Index	A,mm^2	Cma,pF	G, umho	Cco, pF	Const.
6a	Al/Ta2O5/n+Si	586.4	2.072	0.4	960	700	973	16.5
				0.2	480	200	482	16.3
				0.1	250	80	251	17
				0.0225	55	9	55	16.6
6b	Al/Ta2O5/n+Si	576.6	2.082	0.4	1060	780	1075	18.2
				0.2	520	220	522	17.7
				0.1	265	75	265	18
				0.0225	62	9	62	18.7
6c	Al/Ta2O5/n+Si	588.9	2.082	0.4	995	1000	1020	17.3
				0.2	495	175	497	16.8
				0.1	250	60	250	17
				0.0225	57	10	57	17.2
6d	Al/Ta2O5/n+Si	576.1	2.111	0.4	1200	850	1215	20.6
				0.2	600	230	602	20.4
				0.1	310	80	310	21
				0.0225	70	9	70	21

Second annealing temperature:

1. Sample 6a: no annealing
2. Sample 6b: at 420°C
3. Sample 6c: at 600°C
4. Sample 6c: at 750°C

Table 3.2.5. Capacitance, conductance and dielectric constant of MIS (Al/Ta_2O_5/p-Si and Al/Ta_2O_5/n-Si)capacitor, samples 4 and 5, with two-step process vs. electrode areas

Sample	Configuration	Th (A)	Index	A,mm^2	Cma,pF	G, umho	Cco, pF	Const.
4	Al/Ta2O5/p--Si	634.7	2.0762	0.4	1000	400	1004	17
				0.2	500	120	502	17
				0.1	250	40	250	16.9
				0.0225	55	8	55	16.9
5a	Al/Ta2O5/n--Si	583.4	2.0795	0.4	360	2750	892	15.1
				0.2	280	1400	457	15.5
				0.1	190	640	245	16.6
				0.0225	53	70	55	16.6
5b	Al/Ta2O5/n--Si	573.8	2.077	0.4	370	2800	907	15.4
				0.2	310	1560	509	17.3
				0.1	210	640	260	17.6
				0.0225	58	90	62	18.7

Second annealing temperature:

1. Sample 4: at 420°C
2. Sample 5a: no annealing
3. Sample 5b: at 420°C

Fig. 3.2.1. C-V characteristics of Al/20 nm Ta_2O_5/p-Si capacitor with area 0.4 mm^2 at frequency 1 MHz

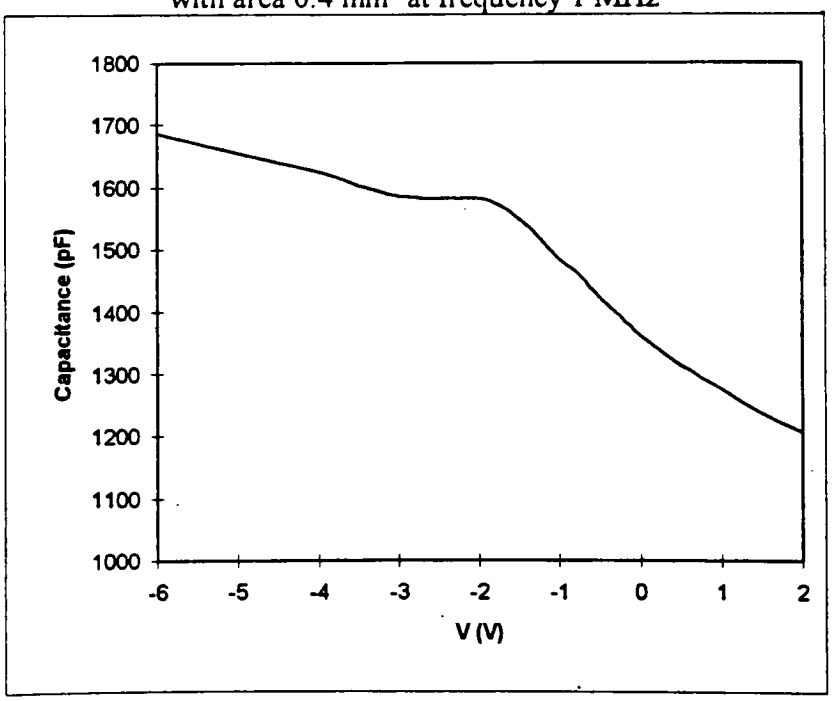


Fig. 3.2.2.C-V characteristics of Al/40 nm Ta_2O_5/n-Si capacitor with area 0.4 mm^2 at frequency 1 MHz

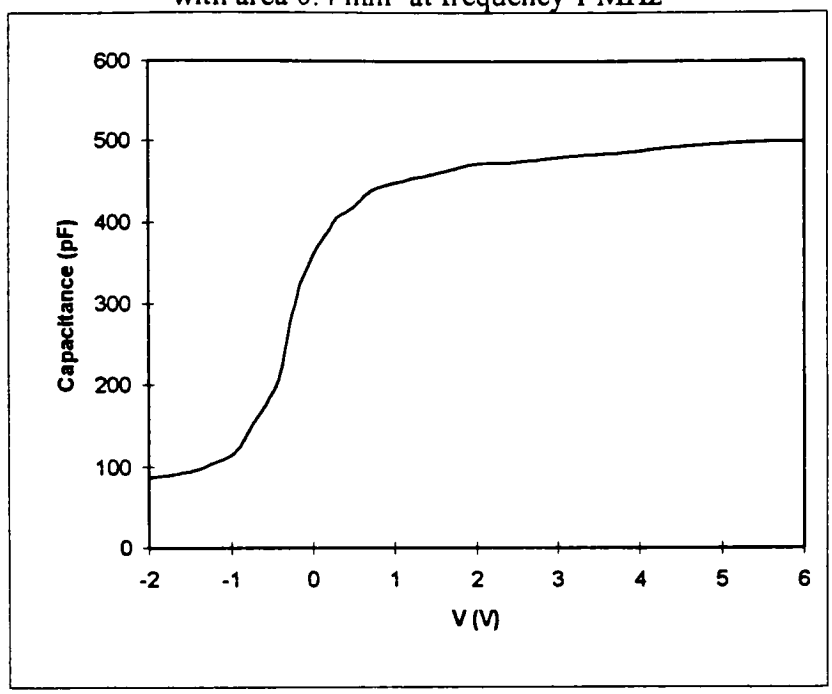


Fig. 3.2.3. Characteristics of leakage current density vs. applied field of Al/20 nm Ta_2O_5/p-Si capacitor

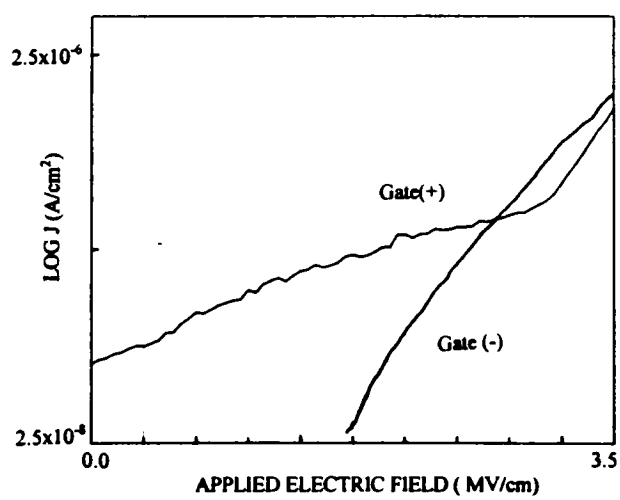


Fig. 3.2.4. Characteristics of leakage current density vs. applied field of Al/40 nm Ta_2O_5/n-Si capacitor

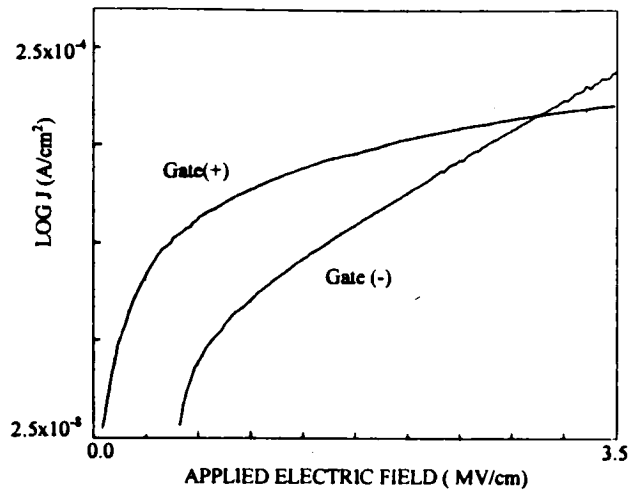
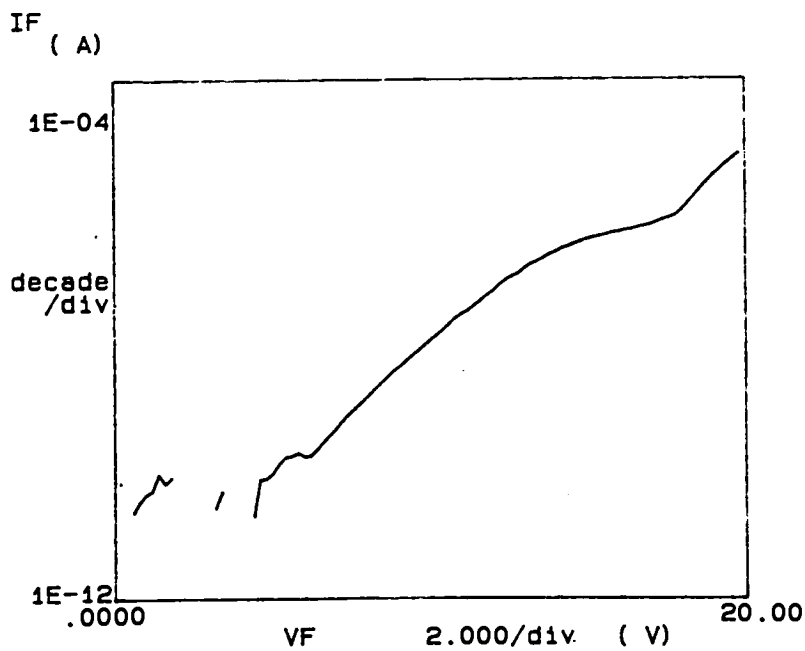


Figure 3.2.5. Characteristics of leakage current vs. applied field of Al/ Ta_2O_5/n+-Si capacitor



3.3. Discussion

The data from Tables 3.2.2. and 3.2.3. are plotted in Figure 3.3.1. in order to show the variation of apparent dielectric constants of as-deposited Ta_2O_5 films among these different substrates, Al film, p-type and n-type silicones. All values are obtained by calculation from capacitance. The capacitor configuration of Al/Ta_2O_5/Al has the highest dielectric constant and the configuration of Al/Ta_2O_5/p-Si has a higher constant than that of A/Ta_2O_5/n-Si. As discussed in Chapter 2, the thinner film has low refractive index because there is a transition layer of Ta_2O_5 between the Ta_2O_5 film and the Si substrate, which has both lower density and refractive index. The contribution weight of lower refractive index for the transition layer to the whole value of refractive index is larger if the film is thin because the relative thickness of the transition layer is larger. As also mentioned in Chapter 1, the higher the refractive index, the higher the dielectric constant. That the value of dielectric constant in the configuration of Al/Ta_2O_5/p-Si is less than that of Al/Ta_2O_5/Al is reasonable because both thickness and refractive index of Ta_2O_5 film in Al/Ta_2O_5/p-Si are less than that in Al/Ta_2O_5/Al. However, the apparent dielectric constant of Ta_2O_5 film in the configuration of Al/Ta_2O_5/n-Si is less than that in Al/Ta_2O_5/p-Si, even though both values of the thickness and refractive index of Ta_2O_5 film in Al/Ta_2O_5/n-Si are larger than that in Al/Ta_2O_5/p-Si. It suggests that the interface or the substrate affects the apparent dielectric constant, especially, the n-type substrate. In other words, the interface or the substrate affects the capacitance. This subject will be discussed further.

Figures 3.3.2. and 3.3.3. show the effect of thermal annealing on deposited Ta_2O_5 film to increase the dielectric constant. The Ta_2O_5 two-step processed film with the

highest annealing temperature, 750°C, has the highest dielectric constant value of 21 with the highest refractive index value of 2.111 as shown in Fig.3.3.2. Comparing this to Fig.3.3.1. the as-deposited Ta_2O_5 film, the Ta_2O_5 films, sample 6a in Fig.3.3.2. and sample 5a in Fig.3.3.3., two-step processed without a second annealing has a higher dielectric constant value of 16. It is clear that the thermal annealing is able to increase the dielectric constant of deposited Ta_2O_5 film.

Thermal annealing is also able to reduce the leakage current of Ta_2O_5 film. Comparing Fig. 3.2.5. to Fig. 3.2.4., the annealed film, sample 6b, has very low leakage current beyond applied field of 1 MV/cm so that HP4145 only picks up noise.

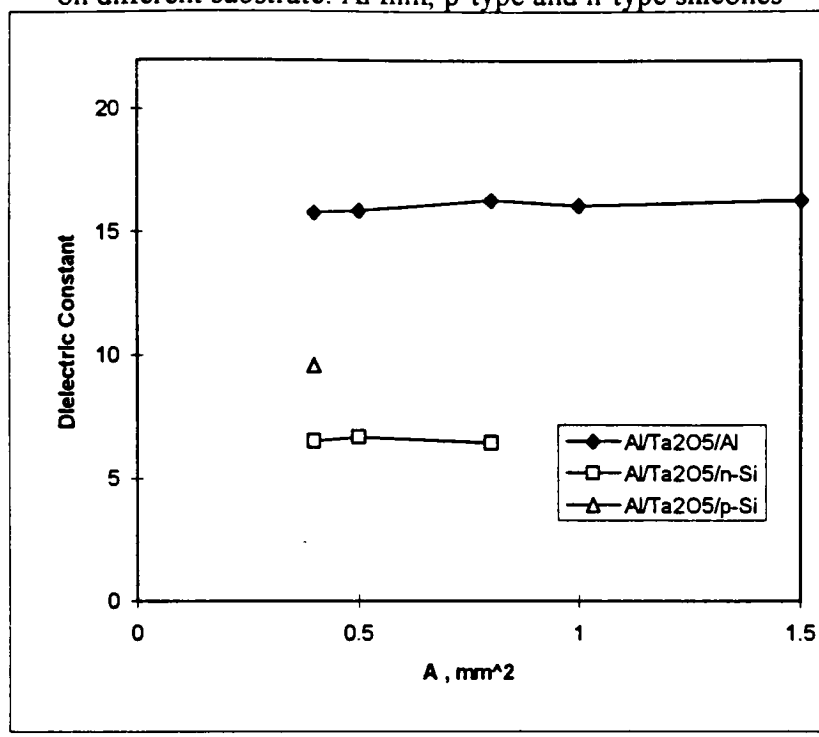
Let us discuss the effect of the interface on the capacitance and leakage current

As discussed in the first paragraph of this section, the capacitor with as-deposited Ta_2O_5 film on the n-type substrate has smaller capacitance and lower dielectric constant than that on the p-type substrate. This same phenomenon is also found in the capacitors fabricated by a two-step process. Comparing all the Tables 3.2.1. to 3.2.5. in section 2, all the capacitances measured are proportional to the electrode areas except the Ta_2O_5 films on the n-type substrate. Figure 3.3.4. shows the measured capacitances of samples 4, 5b, and 6b vs. electrode area on p-type, n-type, and n+-type substrates, respectively. All these films were fabricated by the same process, i.e. first annealing at temperature 700°C and second at 420°C. But the capacitances with the n-type substrate are not proportional to the electrode areas. The reason is that the conductance of capacitors on n-type substrate is the largest.

Figure 3.3.5. shows the conductance of the same capacitors in Fig. 3.3.4. vs. areas. It is found that the capacitor on the p-type substrate, sample 4, has the lowest conductance and the capacitor with n-type substrate, sample 5b, has the highest conductance. The conductance in the C-V measurement represents the leakage current. The lower the conductance, the smaller the leakage current. It suggests to use p-type, p+-type, or n+-type substrates to make DRAM's storage charge capacitors to obtain large capacitance and small leakage current, rather than an n-type substrate.

A model of oxygen deficient in deposited Ta_2O_5 film is proposed to explain the effect of substrate on leakage current. As already mentioned in Chapter 1, it is known that the deposited Ta_2O_5 film is oxygen deficient. Leakage current in Ta_2O_5 film is due to electron carriers. In the accumulation mode of a capacitor with a p-type substrate, the carrier flow, electrons, is from Al side into p-type silicon. It is hard for electrons to over the energy barrier of p-type silicon. However, it is easy for electrons to cross the energy barrier of n-type silicon from silicon side in the accumulation mode. This can explain why the capacitor with p-type substrate has the lowest conductance in the accumulation mode. Then, let us consider different doping on n-type substrate. The conduction band in the n+-type substrate is bent more than that in a n-type substrate, so it is hard for electrons to cross the energy barrier from the n+-type substrate to Al side. This is why the capacitor with n+-type substrate has lower conductance than that with n-type, but higher than that with p-type.

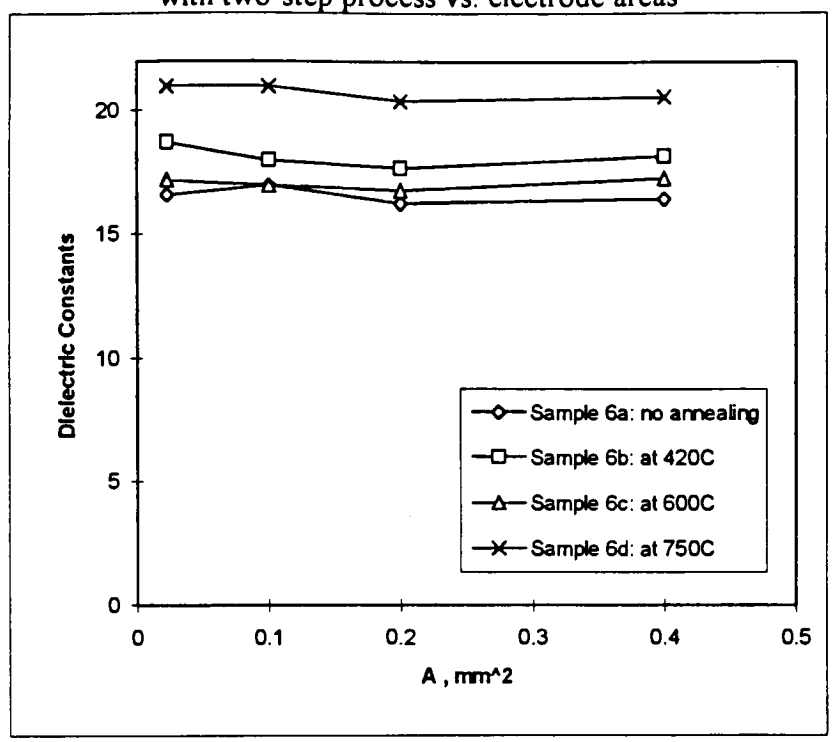
Fig.3.3.1. Apparent dielectric constants of as-deposited Ta_2O_5 film on different substrate: Al film, p-type and n-type silicones



Thickness (A)/refractive index:

1. Sample 1(Al/Ta_2O_5/Al): 1802/2.019
2. Sample 2(Al/Ta_2O_5/p-Si): 214.5/1.737
3. Sample 3(Al/Ta_2O_5/n-Si): 405.6/2.020

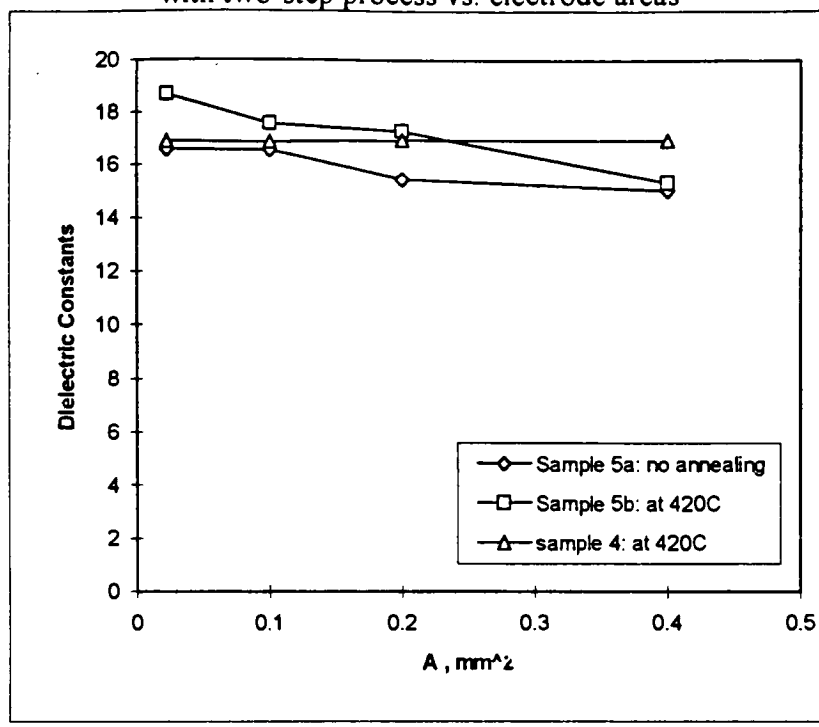
Fig. 3.3.2. Dielectric constants of MIS ($Al/Ta_2O_5/n+-Si$) capacitor with two-step process vs. electrode areas



Thickness (A)/Refractive Index of Sample 6: $Al/Ta_2O_5/n+-Si$

1. Sample 6a: 586.4/2.072
2. Sample 6b: 576.6/2.082
3. Sample 6c: 588.9/2.082
4. Sample 6d: 576.1/2.111

Fig. 3.3.3. Dielectric constants of MIS ($Al/Ta_2O_5/p$-Si and $Al/Ta_2O_5/n$-Si) with two-step process vs. electrode areas



Thickness (A)/Refractive Index:

1. Sample 5a ($Al/Ta_2O_5/n$-Si): 583.4/2.079
2. Sample 5b ($Al/Ta_2O_5/n$-Si): 573.8/2.077
3. Sample 4 ($Al/Ta_2O_5/p$-Si): 634.7/2.067

Figure 3.3.4. Capacitance vs. electrode area on different substrate

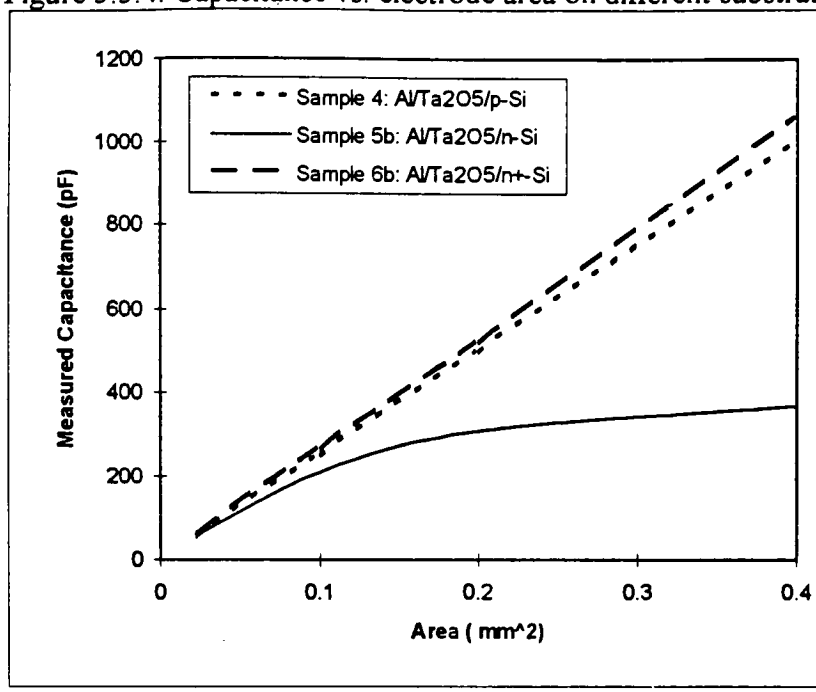
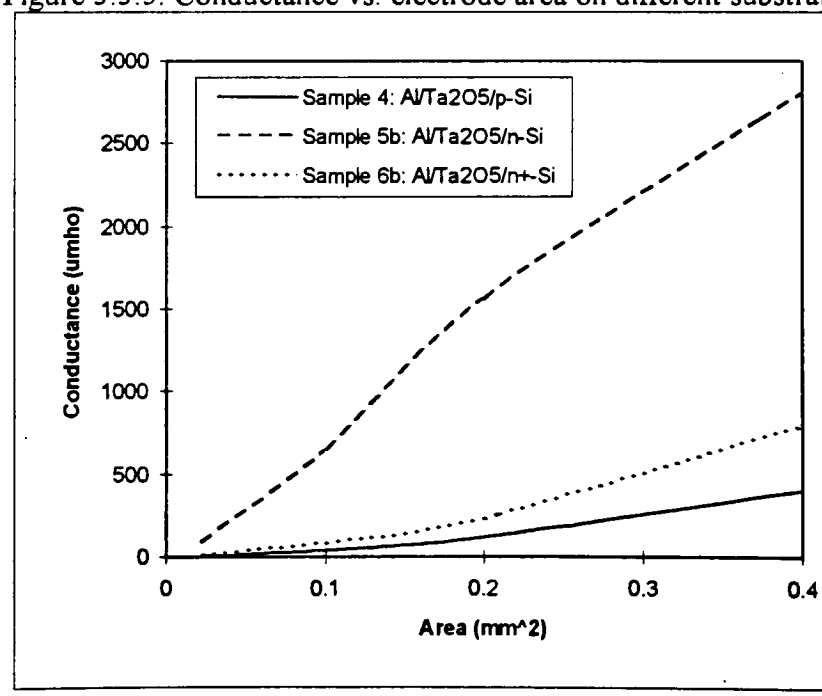


Figure 3.3.5. Conductance vs. electrode area on different substrate



Reference

[1] E.H. Nicollian and J.R. Brews, "MOS Physics and Technology," Wiley Press, c1982

Chapter 4. Optical Absorption of Tantalum Oxide Thin Films

4.1. Experimental

The scanning uv-vis spectrophotometry, model PE 552A, was used to explore the optical absorption of prepared tantalum oxide thin films. The PE 552A is a double beam, microcomputer controlled scanning spectrophotometer. The wavelength range is 900 nm to 190 nm, i.e. ir to uv. The measurement was set up as Response time = 0.5 sec, Slit = 0.25 nm, Scan speed = 20 nm/min, Record speed = 5 nm/min, and Mode = Absorbency.

The samples used for spectrophotometer were as-deposited, furnace annealed, and uv-beam laser annealed Ta_2O_5 films. The Ta_2O_5 film was deposited on quartz with thickness of 1800 A using DC active sputter, the CVC-601. In order to study the effect of phase transformation from amorphous to crystalline on the absorbency spectrum of Ta_2O_5 film, furnace annealing and uv-laser beam annealing were utilized to treat as-deposited films.

The quartz sample in the reference beam was of the same quality as that used for substrate.

4.2. Absorbency of UV-VIS Spectrum in Ta_2O_5 Films

4.2a. As-deposited Films

The spectrum of the as-deposited Ta_2O_5 film revealed two main absorbency peaks and one subpeak as shown in Figure 4.2.1. The wavelengths of main absorbency peaks,

named as peak 1 and peak 2, are 217 nm and 416 nm, respectively. The peak 1 with wavelength of 217 nm in UV region has higher absorbency than peak 2 at 416 nm. The peak 1 has a subpeak at 286 nm, named as subpeak 1.

4.2b. Furnace Annealed Films

Both the as-deposited Ta_2O_5 film with quartz substrate and the reference quartz sample used for spectrophotometer were annealed in thermal furnace for 30 min at temperature of 800°C in oxygen ambient. The annealed Ta_2O_5 film was measured by the spectrophotometer. The absorbency spectrum of Ta_2O_5 film shows that peak 1 and peak 2 are still present, but subpeak 1 disappeared and the peak 2 became narrower as shown in Figure 4.2.2.

4.2c. Laser Annealed Films

A laser beam with a wavelength of 193 nm was used to anneal as-deposited Ta_2O_5 film on quartz. The energy density of laser beam of 193 nm was calibrated as 30 mJ/cm^2*pulse. Then the as-deposited Ta_2O_5 film on quartz was laser treated. A shadow with the same shape as the Ta_2O_5 film appeared on a screen set behind the film. That means the Ta_2O_5 film strongly absorbs the laser beam with wavelength of 193 nm, but the quartz is transparent for this laser. In other words, the Ta_2O_5 film is able to absorb all the energy of laser beam to treat itself. This is consistent with the spectrophotometer result.

Films exposed to 20, 200, and 2000 pulses in the laser beam showed no change in the absorbency spectrum compared with as-deposited Ta_2O_5 films.

Fig. 4.2.1. UV-VIS absorbency spectrum of as-deposited Ta_2O_5 film

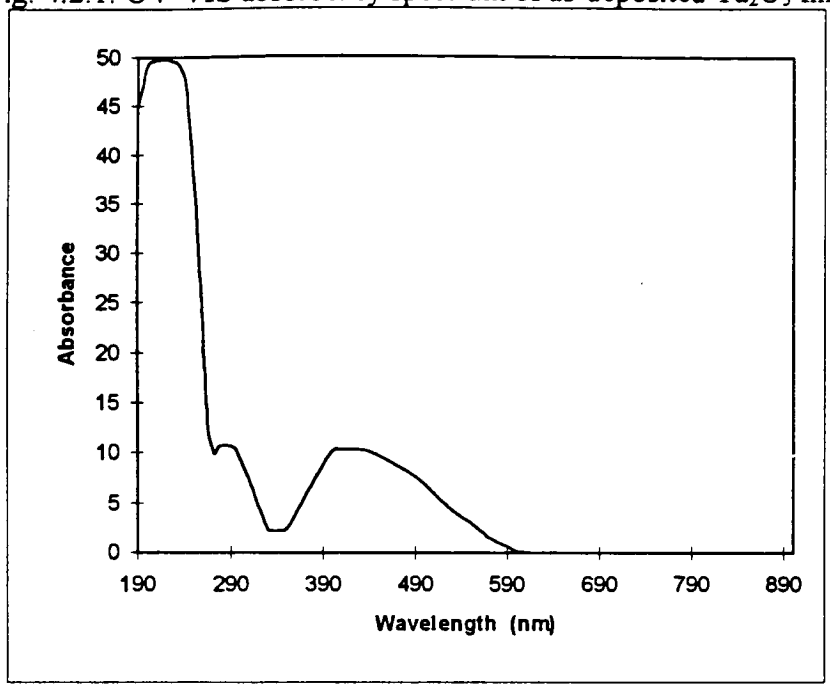
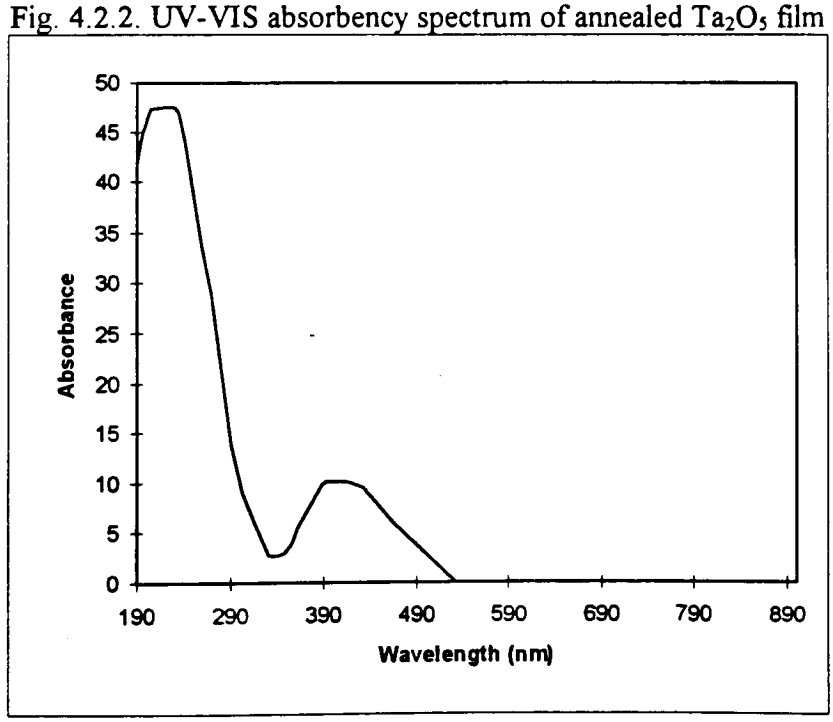


Fig. 4.2.2. UV-VIS absorbency spectrum of annealed Ta_2O_5 film



4.3. Discussion

Let us analyze the change of absorbency spectrum of Ta_2O_5 film after annealing. The absorbency spectrum of the as-deposited Ta_2O_5 film is overlapped on that of the annealed film in Figure 4.3.1. The valleys at 330 nm match precisely. Peak 1 at 217 nm broadens and subsumes the subpeak, and the long wavelength side of peak 2 drops considerably making peak 2 narrower. The difference between the two spectra in the region of peak 2 shows that peak 2 in the as-deposited film can be considered as the combination of peak 2 with a subpeak 2 as shown in Figure 4.3.1.

As discussed in Chapters 1 and 2, the as-deposited Ta_2O_5 film is in amorphous state while the annealed film is in crystalline state. The amorphous film can be condensed during annealing. It is well known that the structure of the amorphous state is described in terms of the short range order and long range disorder, or the free volume. On the other hand, in the theory of crystal field in terms of group theory and symmetry representation [1], if a defect is introduced into symmetric crystal structure, the degree of symmetry of the group will reduce and the crystal field will split. If the position of defect is different in the crystal structure, the splitting of crystal field will change.

The annealing effect on absorbency spectrum of Ta_2O_5 film can be explained from a solid state physics point of view. It suggests that the crystal field of Ta_2O_5 film has two excited energy levels, corresponding to peak 1 and peak 2. Subpeak 1 and subpeak 2 are due to crystal field splitting. In the amorphous state, i.e. as-deposited Ta_2O_5 film, the free volume could be considered as a vacancy defect to split the crystal field. After annealing,

the free volume is released from the structure and subpeak 2 disappeared from the absorbency spectrum. It suggests that the free volume contributes to subpeak 2.

As discussed in Chapters 1 and 3, the mechanism of leakage current of Ta_2O_5 film is due to oxygen vacancy. There is still leakage current in Ta_2O_5 film after annealing. It suggests that the defect of oxygen vacancy contributes to subpeak 1.

The Bohr-Einstein frequency relationship is used to calculate energy for each peak with results listed in Table 4.3.1.

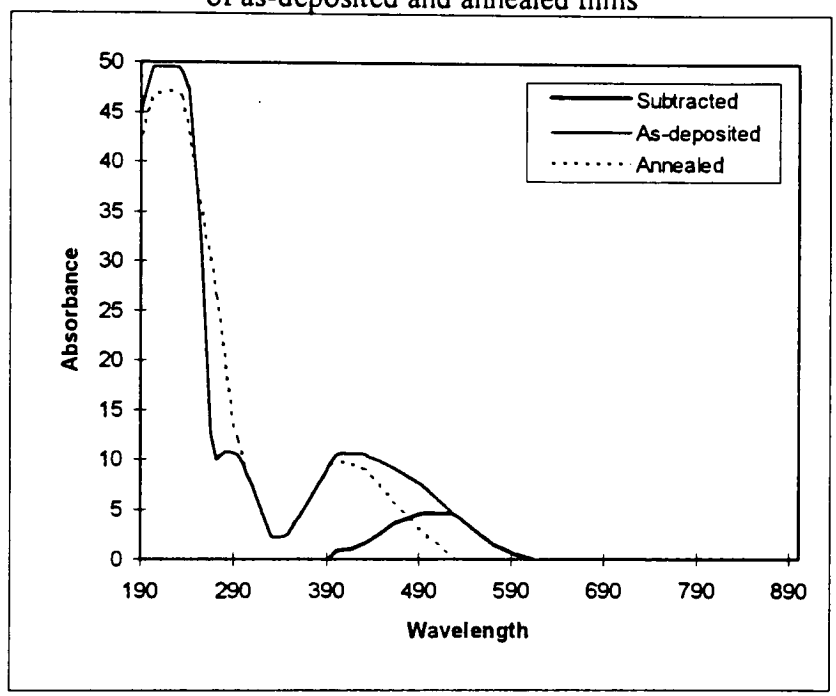
In summary, there are two kinds of defects in Ta_2O_5 film, an oxygen vacancy-like defect and a free volume-like defect, which locate in different positions of structure and contribute to subpeak 1 and subpeak 2 in absorbency spectrum, respectively. In as deposited Ta_2O_5 film, the free volume-like defect contributes to subpeak 2 so that the peak 2 in Figure 4.2.1 is a combination of annealed peak 2 and subpeak 2. In annealed Ta_2O_5 film, the oxygen vacancy-like defect contributes to subpeak 2 so that the subpeak 1 merges with peak 1 as shown in Figure 4.2.2.

There is no change of absorbency spectrum of Ta_2O_5 film after 2000 pulses of laser annealing at 193 nm. The calculation shows the temperature of Ta_2O_5 film may increase to very high if we assume the film absorbs all of the energy of laser beam. The frequency of pulse is 20 pulses per second. It suggests that the film temperature decreases in the period between two pulses so that the final temperature after pulse may not be high enough to anneal the Ta_2O_5 film.

Table 4.3.1. Wavelength and energy of absorbency peaks in Ta_2O_5 films

Peak	Wavelength	Energy, eV
peak 1	217 nm	5.7
subpeak 1	286 nm	4.3
peak 2	416 nm	3.0
subpeak 2	510 nm	2.4

Fig. 4.3.1. Overlap of absorbency spectrum of as-deposited and annealed films



Reference

[1] Boris S. Tsukerblat, " Group theory in chemistry and spectroscopy," Academic Press, 1994.

Chapter 5. Etching of Tantalum Oxide Thin Films

5.1. Wet Etching

Wet etching was studied first. It has been reported that tantalum and tantalum compounds can be etched in HF, and that Ta_2O_5 does not etch as rapidly as TaN and Ta. Therefore, the Ta_2O_5 acts as a protector for the substrate surface. However, it is difficult to etch tantalum compounds in HF if the substrate is silica. It has also been reported that the tantalum and Ta_2O_5 can be etched in heated KOH solution.

5.1a. Experimental

Three kinds of samples, Ta film on silicon, Ta_2O_5 film on silicon, and $Ta/Ta_2O_5/Ta$ triple layers on silicon, were prepared for wet etching experiment. All the films were deposited with the CVC-601 DC sputter equipment. The thickness of Ta was 3000A and the thickness of Ta_2O_5 was 1800A.

Solutions of HCl, NaOH and KOH, were used for wet etching. The solution of HCl were 37% or 20% of concentration, respectively, by volume at room temperature. The NaOH solution was heated to 45°C which is the standard method used for Aluminum etching in the RIT Fab. The KOH solution was made up of 30% sodium (or potassium) hydroxide and 30-35% hydrogen peroxide by volume [1]. The proportion was about 9 or 10 to 1 of NaOH to H_2O_2 . The solution with KOH only was heated to 90°C, then the H_2O_2 was added.

Microscope was used to observe the etched wafer surface to identify the usefulness of hot KOH etching.

5.1b. Results and Discussion

The sample of Ta/Si with 3000A Ta film withstood both 37% HCl and 20% HCl at room temperature for 30 min without change. The sample surface was still shiny. There was no visible evidence to show that the Ta film was etched. It also withstood the NaOH solution at 45 °C for 30 min, and there was no change to the surface.

The heated KOH solution etched the samples of Ta/Si, Ta_2O_5/Si and Ta/Ta_2O_5/Ta/Si. Two photos of the microscope were token focusing on the edge of the films after etching. Fig. 5.1.1. of a microscope photo illustrates a sample of Ta_2O_5/Si which was etched for 3 min in KOH solution. It shows that there is a trenched line in the silicon side just by the edge of the Ta_2O_5 film so that the silicon has been etched enough to reveal the characteristic KOH etch surface feather. Fig. 5.1.2. shows the sample of Ta/Si which was etched for 5 min in KOH solution. This also shows a trenched line in the silicon side just by the edge of the Ta film. This line is wider and deeper than that in the Ta_2O_5/Si sample in Fig. 5.1.1 because the etching time was longer. The right hand side on the wafer in this picture was covered by the Ta film before being etched. After etching, the Ta film had been completely removed, except that a very thin line of the Ta film remained at the edge. The right band side of this Ta line is not smooth. This suggests that there was an elector-chemical cell consisting of Si and Ta, in which the silicon cathode was etched and the Ta anode was protected in the region at the Ta/Si boundary. But the Ta film was piled

because the silicon under the Ta film was etched. Fig. 5.1.3. shows the sample of $Ta/Ta_2O_5/Ta/Si$ after etching for 1.5 min in KOH solution. It shows that the $Ta/Ta_2O_5/Ta$ film was piled at the beginning of etching. It also suggests that the only silicon was easily etched rather than Ta film.

In summary, hot KOH is not suitable for etching Ta and Ta_2O_5 films. In the case of the Ta/Si system, first, the Ta film can be piled, but not be etched. Secondly, the edge of the Ta film remains after etching. Finally, a trenched line on the silicon side by the edge of the Ta film is produced. This edge sensitively to etching suggests an electro-chemical cell effect. In the case of the Ta_2O_5/Si system, there will also be a trenched line on the silicon side by the edge of the Ta film. No useful selectivity of both Ta and Ta_2O_5 films to silicon substrate was observed with the wet etching solution studies.

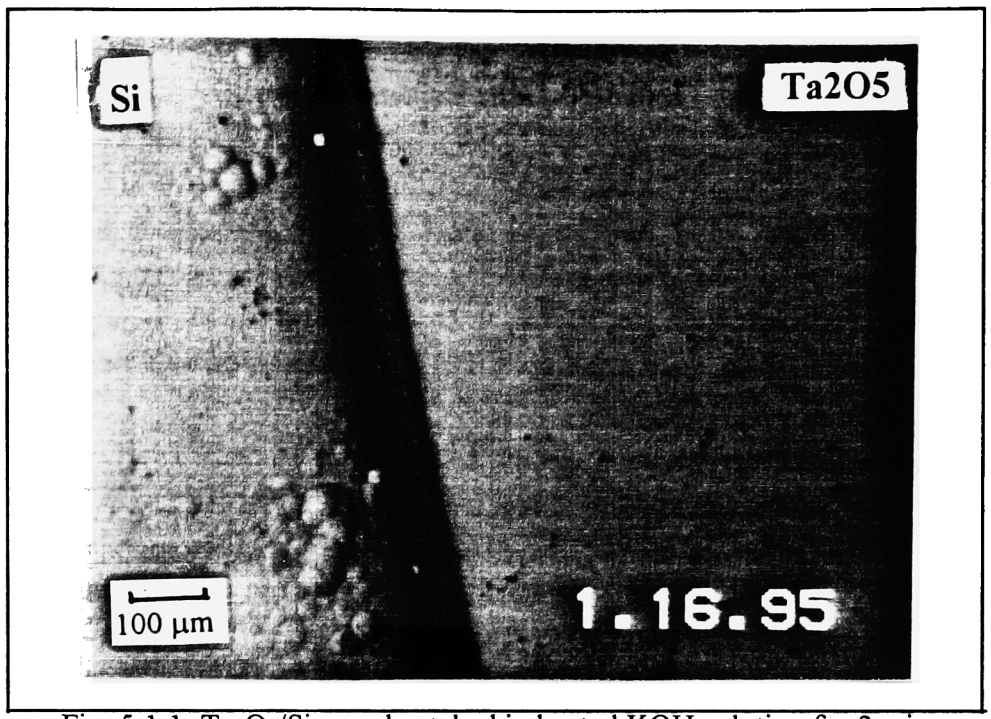


Fig. 5.1.1. Ta_2O_5/Si sample etched in heated KOH solution for 3 min using microscope at 100x

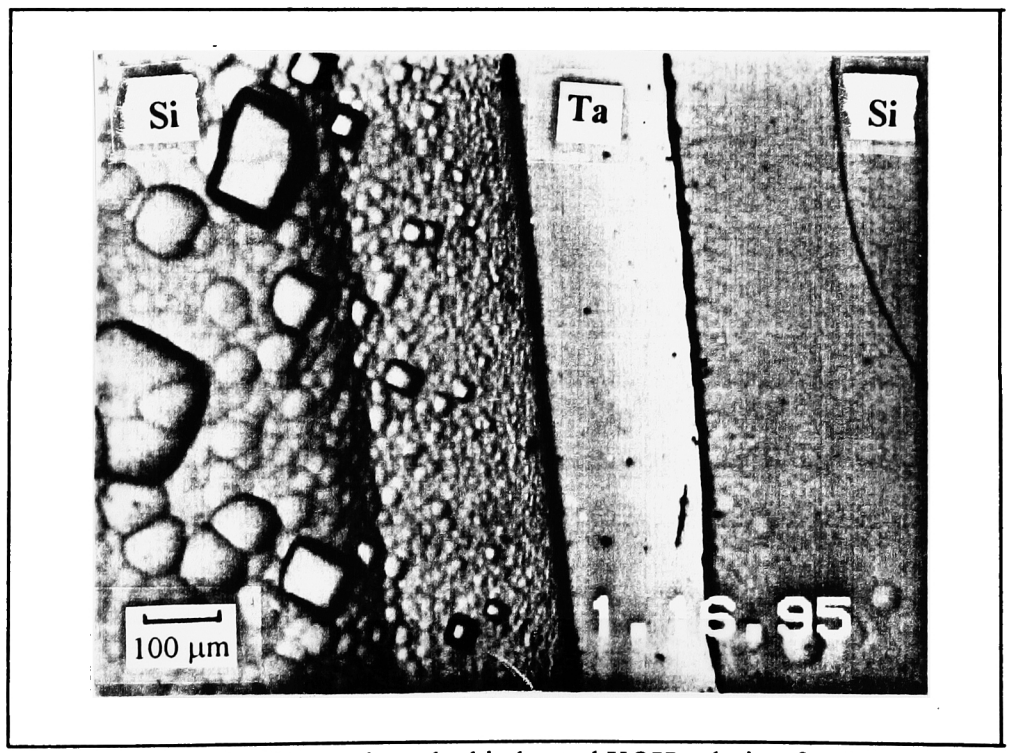


Fig. 5.1.2. Ta/Si sample etched in heated KOH solution for 5 min using microscope at 100x

Fig. 5.1.3. $Ta/Ta_2O_5/Ta/Si$ sample etched in heated KOH solution for 1.5 min using microscope at 100x

5.2. Dry Etching

The wet etching of the samples in the heated KOH solution has revealed that there is an electro-chemical cell effect in the silicon-tantalum system, with the result that wet etching is not suitable for etching of both Ta and Ta_2O_5 on a silicon substrate. Dry etching characteristics of tantalum and tantalum oxide were therefore explored. Samples were prepared by depositing combinations of Ta_2O_5, Ta, polysilicon, and SiO_2 films on silicon wafers. RIE-etching experiment were prepared using etching gases of CHF_3, CF_4, and SF_6, as well as mixtures of CF_4-O_2 , CF_4-H_2, SF_6-H_2, and SF_6-Ar. Etch rates and selectivities were determined.

5.2a. Sample Preparation

In order to study the etching selectivity of Ta_2O_5 to Ta, poly-Si, and SiO_2 , four films were deposited onto a wafer. Fig 5.2.1. shows the typical film configuration.

The sample preparation process was as following:

1. RCA cleaning
2. Thermal Oxidation of SiO_2 film for 5000A in dry O_2 at 1100°C for 30 min
3. Photoresist coating on the front side of wafer on WaferTrac
4. Wet etching the backside SiO_2 in BOE to remove oxide
5. Photoresist stripping in Asher
6. Photoresist coating front side
7. Exposing and developing the left half of the wafer

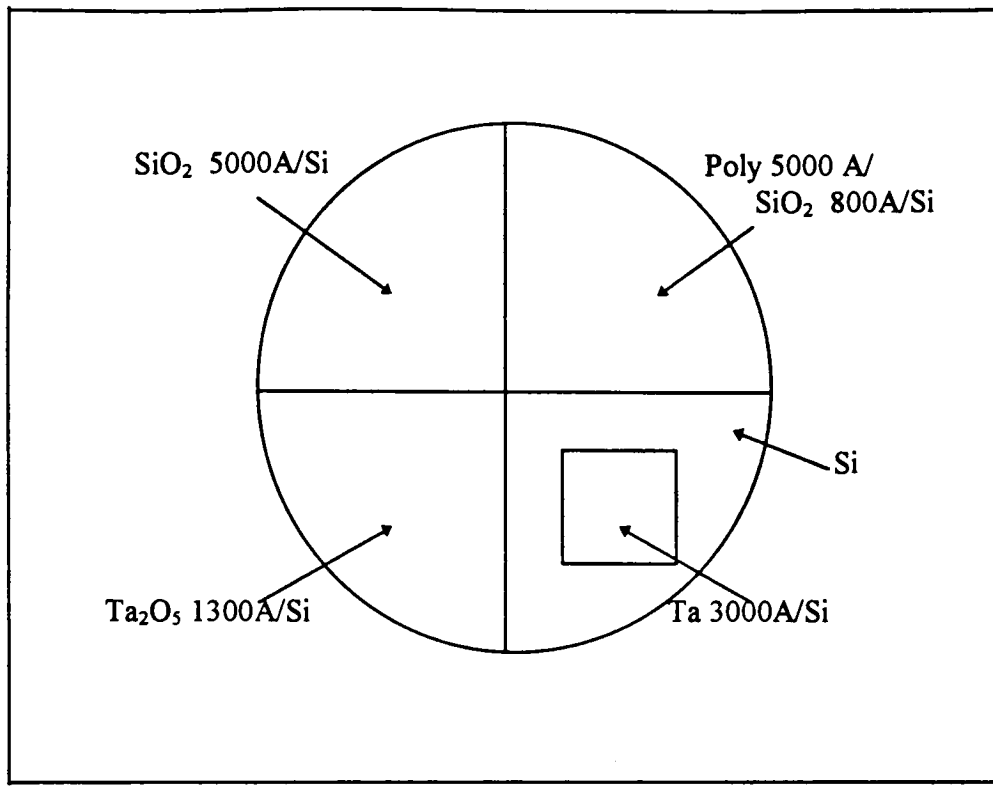


Fig. 5.2.1. Film configuration of Ta, Ta_2O_5, poly-Si, and SiO_2

8. Wet etching the oxide on the left half wafer in BOE for 4 min to obtain 800A SiO_2 thickness
9. Photoresist stripping in Asher
10. RCA cleaning
11. Depositing a 5000A polysilicon in LPCVD at 605°C for 65 min
12. Photoresist coating
13. Masking the upper left quarter of polysilicon and exposing and developing remaining three quarters of wafers
14. Wet etching, removing the polysilicon on three quarters of the wafers

15. Wet etching in BOE, removing the SiO_2 on the lower half of wafers

16. Photoresist stripping in Asher

17. Masking and DC reactive sputtering Ta_2O_5 on the lower left quarter of wafers

18. Masking and sputtering Ta on the lower right quarter of wafers.

The process conditions for film deposition were as follows:

1. Thermal oxidation of 5000A SiO_2 : dry O_2 , 5 slpm, 1100°C, 30 min.
2. LPCVD deposition of 5000A poly: 605°C, 288 mTorr, 65 min, 90 sccm, saline: N_2=0.45:0.55.
3. DC sputter deposition of Ta_2O_5:Ar:O_2 =0.80:0.20, 5.8 mTorr, 450V, 1.2A, 60 min.
4. DC sputter deposition of Ta: Ar: 4.5 mTorr, 330V, 8.0A, 30 min.

The wet etching rate of polysilicon was found to be 1550 A/min in the solution with HNO_3 64%, D.I. 33%, and BOE 3% by volume.

5.2b. Experimental

Dry etching was carried out by using the Reactive Ion Etch (RIE). In the first stage of the experiment, the CHF_3 and CF_4 with additions of H_2 or O_2 up to 30% were chosen as etching gases. The fractions of O_2 were 6, 8, 15, 20, 25, and 30%. The fractions of H_2 were 10, 20, and 30%. The power was 150 W, the pressure was 20 mTorr, and the total flow rate was 50 sccm. Table 5.2.1a lists the experiment conditions of CH_4 etching. Each sample was etched for 10 min. Thickness measurement was made after each minute

etching for the first six minutes. Final thicknesses were measured after last four minute etch. The etch rates were determined using the data of the first six minutes.

Table 5.2.1a. Fractions of H_2 or O_2 in CF_4 etching

CF4:O2	0.94:0.06	0.92:0.08	0.85:0.15	0.80:0.20	0.75:0.25	0.70:0.30
CF4:H2	0.90:0.10	0.80:0.20	0.70:0.30			

Power: 150 W
Pressure: 20 mTorr
Flow Rate: 50 sccm

Table 5.2.1b. Pressure, flow rate and fractions of H_2 or Ar in SF_6 etching

Gas	Pressure mTorr	Flow Rate sccm
SF_6	50	80
	150	80
	150	200
SF_6:H_2 0.8:0.2	50	80
	150	80
	150	200
SF_6:Ar 0.8:0.2	50	120
	150	120
	150	200

The result of the initial experiment was that Ta_2O_5 did not etch faster than SiO_2 or poly. So the etch gas of SF_6 was chosen for a second experiment. The reason was that it had been reported that the etch rate of Ta film in the etch gas of SF_6 was as high as 1 μm/min [2]. In this experiment, the etch gas of SF_6 with addition of the H_2 or Ar were used. The power was 150 W. The pressure and the flow rates changed from 80 to 200 mTorr, and from 50 to 150 sccm, respectively, as shown in Table 5.2.1b. The etch time was 2 min for each sample and the film thicknesses were measured with the Nanospec.

5.2c. Results

The thicknesses of Ta_2O_5, SiO_2 , and polysilicon films versus time in the RIE with the various etching gases are show in Tables. These results are also plotted as shown in Figs. of 5.2.2. to 5.2.12, respectively. The RIE etch rates of Ta_2O_5, SiO_2 , and polysilicon in CHF_3 and the gas mixtures of CF_4 with up to 30% O_2 and H_2 are listed in Table 5.2.2. Fig. 5.2.13. shows the variations of etching rates in CF_4 for various amount of O_2 and H_2. Fig. 5.2.14. shows the variations of the etching rate in CF_4 for various amount of H_2 compared to pure CHF_3.

Table 5.2.3. shows the etching rates of Ta_2O_5, Ta, SiO_2 , and poly films in SF_6 with up to 30% Ar and H_2.

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	5023	4848	1339
1	4527	4424	1169
2	4163	4240	1086
3	3670	3861	912
4	3221	3592	787
5	2897	3381	689
6	2575	3224	642
10	989	2208	143

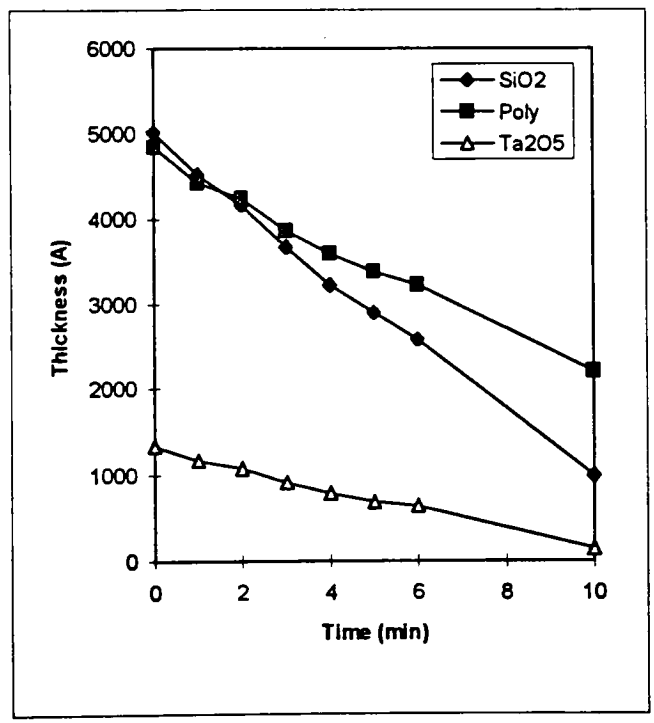


Fig. 5.2.2. Thicknesses of films versus time in CF_4

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	5010	5235	1338
1	4583	5123	1210
2	4204	4807	1106
3	3851	4567	959
4	3473	4323	896
5	3064	3985	762
6	2626	3638	642
10	540	1813	50

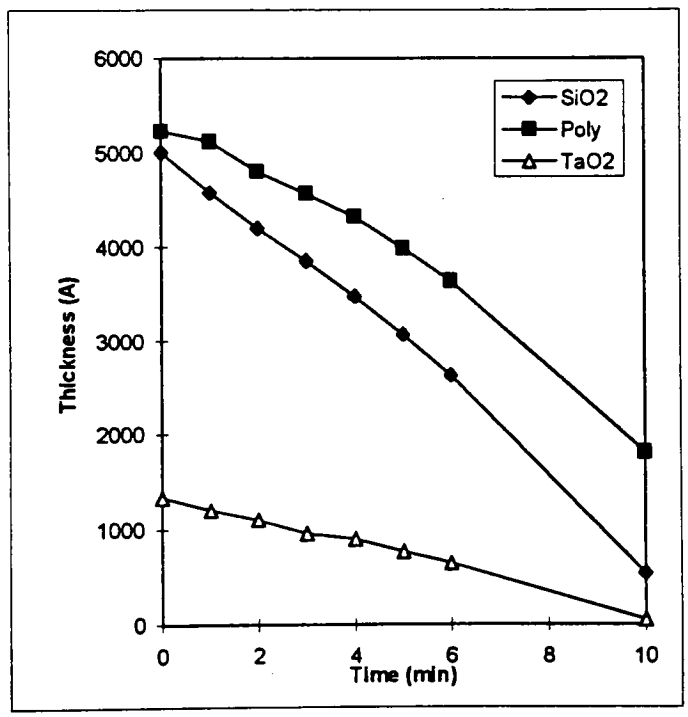


Fig. 5.2.3. Thicknesses of films versus time in CF_4 with 6% O_2

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	5017	5220	1255
1	4539	4890	1059
2	3947	4356	887
3	3634	4312	798
4	3286	4068	698
5	2945	3856	631
6	2550	3692	550
10	798	2535	0

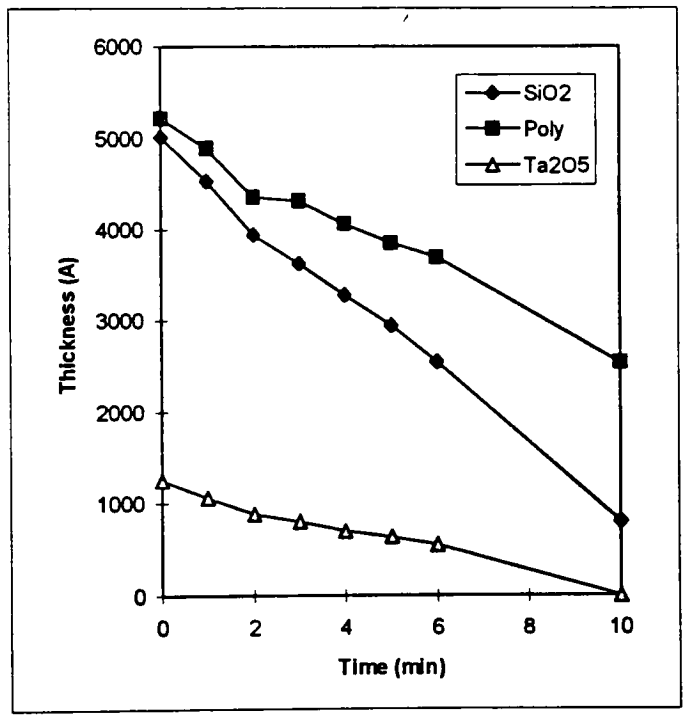


Fig.5.2.4. Thicknesses of films versus time in CF_4 with 8% O_2

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	5014	5296	1148
1	4528	5040	1083
2	4220	4851	1015
3	3896	4561	942
4	3532	4291	829
5	3141	4107	743
6	2728	3918	589
10	823	2510	0

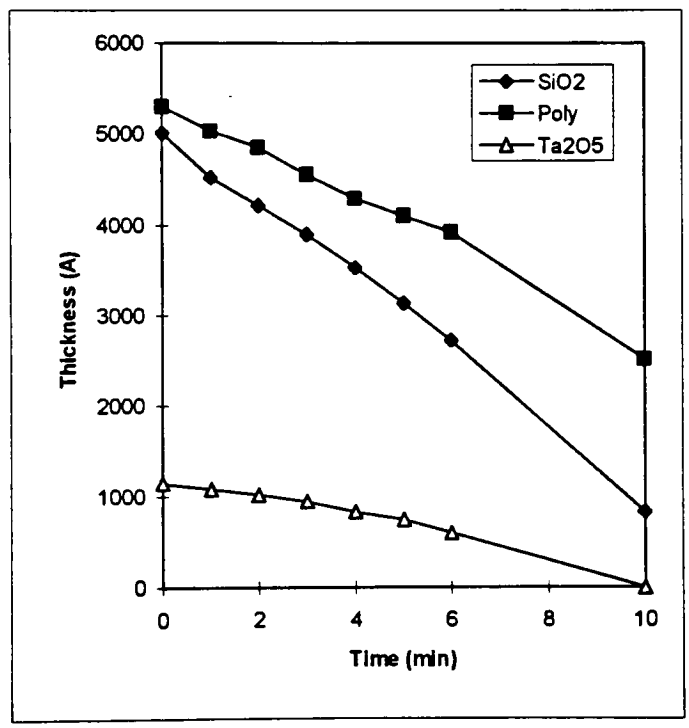


Fig. 5.2.5. Thicknesses of films versus time in CF_4 with 15% O_2

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	4946	4935	1265
1	4454	4670	1073
2	3920	4188	878
3	3624	4187	799
4	3290	3867	694
5	2976	3641	626
6	2663	3380	564
10	1020	2356	50

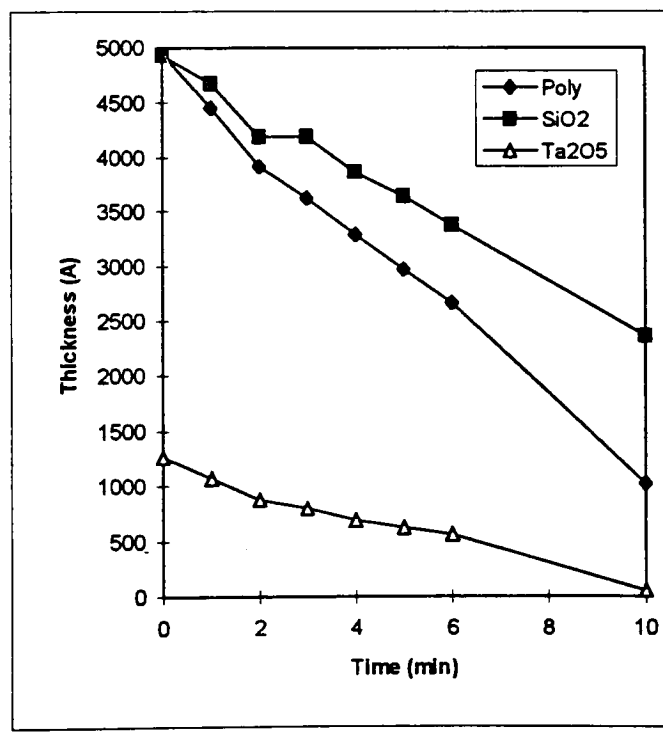


Fig. 5.2.6. Thicknesses of films versus time in CF_4 with 20% O_2

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	4996	5169	1354
1	4480	4811	1146
2	4177	4700	1077
3	3863	4521	991
4	3533	4370	907
5	3162	4212	801
6	2821	4067	697
10	1212	3189	100

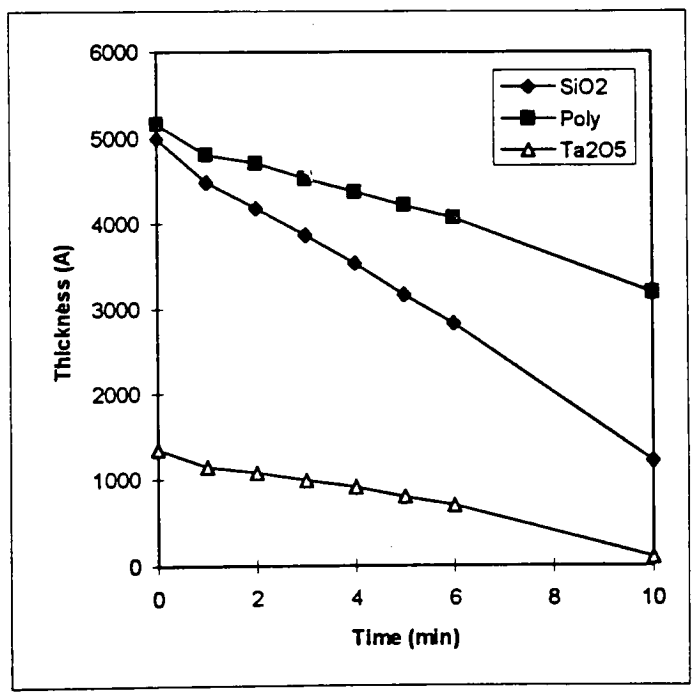


Fig.5.2.7. Thicknesses of films versus time in CF_4 with 25% O_2

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	4987	5191	1331
1	4662	4926	1232
2	4340	4889	1135
3	4070	4650	1055
4	3808	4473	997
5	3570	4387	921
6	3313	4251	872
10	2260	3593	517

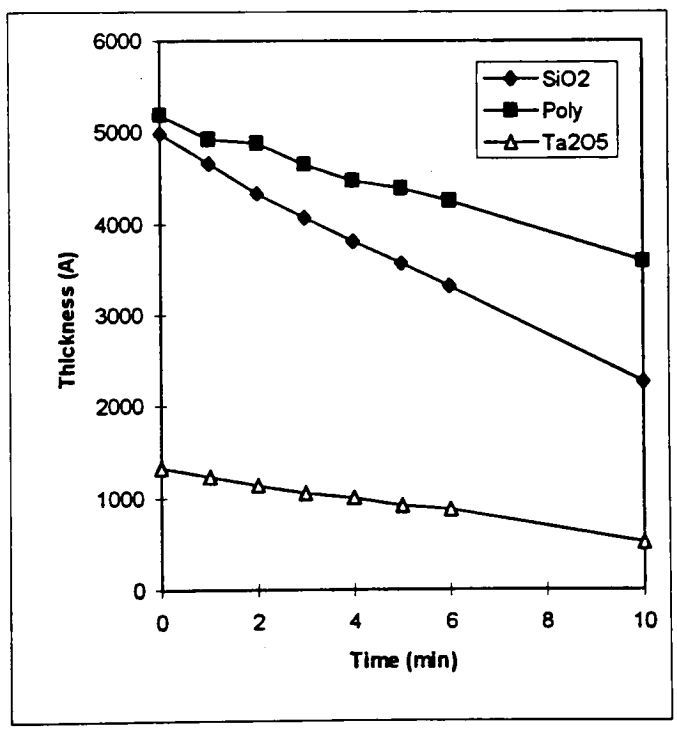


Fig. 5.2.8. Thicknesses of films versus time in CF_4 with 30% O_2

Time (min)	SiO2 (A/min)	Poly (A/min)	Ta2o5 (min)
0	3986	4402	903
1	3690	4224	864
2	3437	4007	803
3	3162	3803	743
4	2845	3551	682
5	2545	3518	632
6	2294	3281	595
10	1165	2589	315

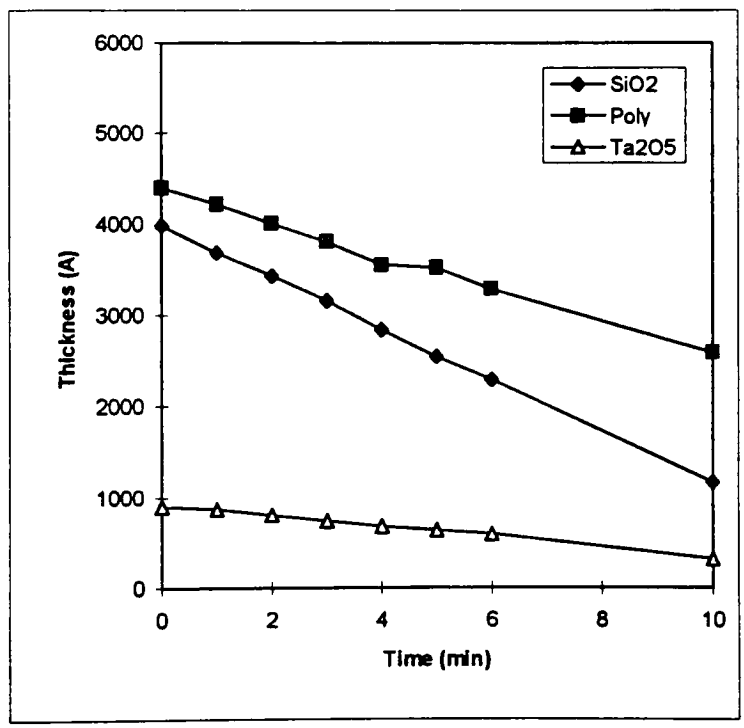


Fig. 5.2.9. Thicknesses of films versus time in CF_4 with 10% H_2

Time (min)	SiO2 (A)	Poly (A)	Ta2O5 (A)
0	5010	5162	1348
1	4608	4911	1231
2	4249	4688	1173
3	3941	4513	1104
4	3639	4292	1039
5	3348	4158	980
6	3067	4052	919
10	1685	3175	616

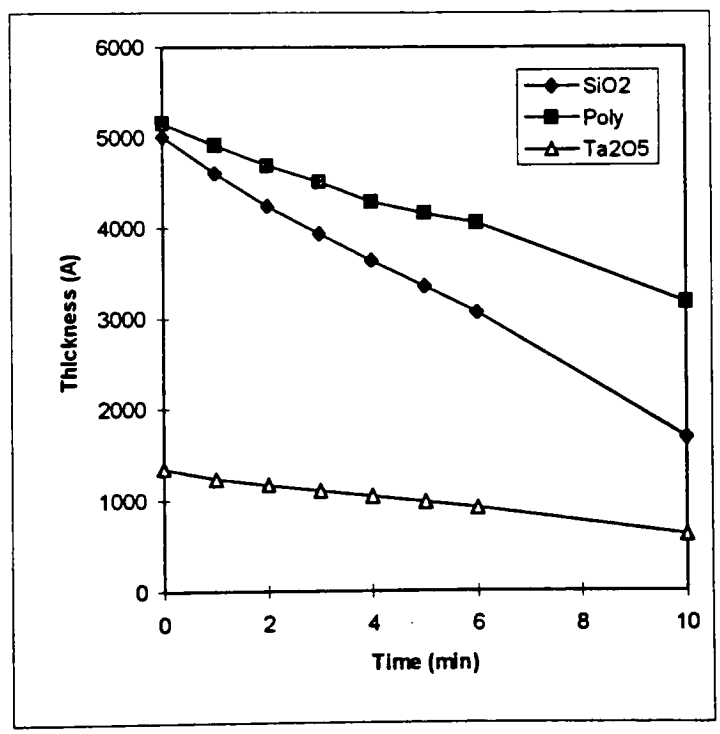


Fig. 5.2.10. Thicknesses of films versus time in CF_4 with 20% H_2

Time (min)	SiO2 (A)	Poly (A)	Ta2O5 (A)
0	4976	4865	1334
1	4779	4751	1287
2	4532	4628	1238
3	4366	4545	1191
4	4194	4438	1150
5	3999	4355	1105
6	3780	4235	1047
10	3080	3882	880

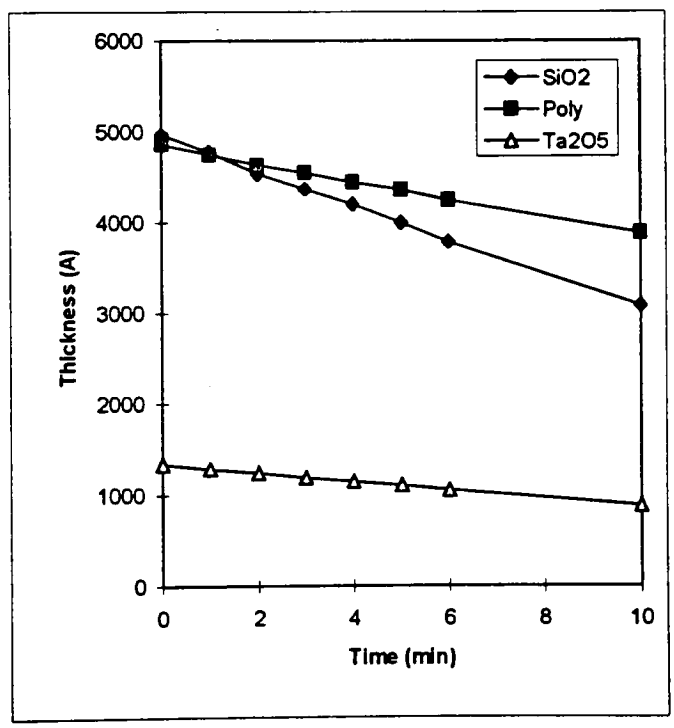


Fig. 5.2.11. Thicknesses of films versus time in CF_4 with 30% H_2

Time (min)	SiO2 (A)	Polysilicon(A)	Ta2O5 (A)
0	5009	5066	1244
1	4564	4965	1169
2	4104	4857	1109
3	3675	4755	1071
4	3262	4650	945
5	2819	4539	871
6	2401	4430	814
10	596	4190	292

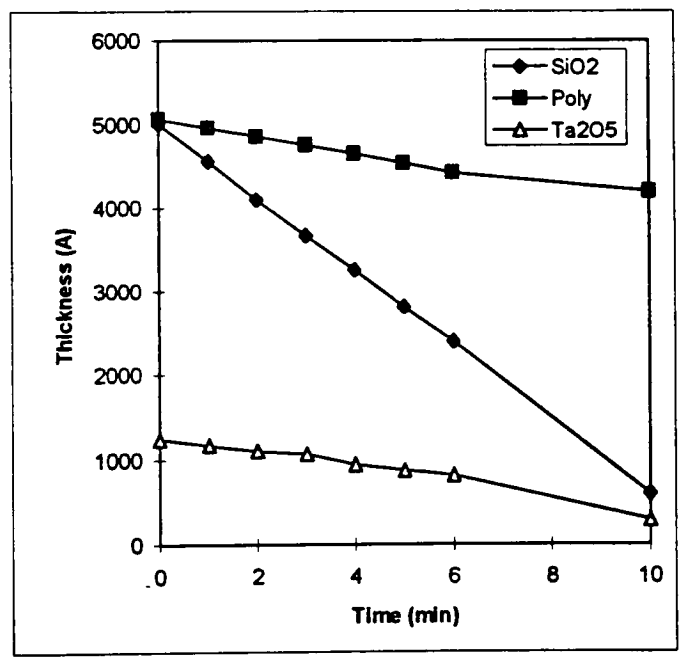


Fig. 5.2.12. Thicknesses of films versus time in CHF_3

5.2d. Discussion

Fig. 5.2.13. reveals that the etching rates of Ta_2O_5 film are always slower than that of SiO_2 and poly in CF_4 gas, even though either O_2 or H_2 is added. The variations of etching rates of SiO_2 and polysilicon in CF_4 with O_2 or H_2 addition are similar to these reported elsewhere [1]. On the O_2 side, the etching rates of SiO_2 and polysilicon increase with increasing concentration of O_2 , reaches the maximum value in the range of 10~20%, then, decreases. This can be explained by the model of F/C ratio. While the fraction of oxygen increases, the carbon and oxygen atoms can form CO or CO_2 to increase the ratio of F/C and thereby increase the etching rate. On the H_2 side, however, both the etching rates of SiO_2 and polysilicon decrease monotonically. The etching rate of Ta_2O_5 does not change greatly with O_2 addition except 30% O_2 but the etching rate drops significantly by adding H_2. That the etching rate of Ta_2O_5 is always lower than SiO_2 and poly in CF_4 with O_2 and H_2 suggests that the physical etching is a main mechanism for Ta_2O_5 rather than chemical etching.

Fig. 5.2.14. reveals that the best selectivity of Ta_2O_5 to poly is the use of CHF_3. One concludes that CHF_3 should be chosen if a window or contact cut will be open on the Ta_2O_5 film with a silicon substrate. This figure also reveals that the selectivity of SiO_2 to poly in the etching gas of CHF_3 is better than that of CF_4 with H_2 addition. Some reports revealed that adding H_2 in CF_4 can increase the selectivity of SiO_2 to polysilicon [1]. Fig. 5.2.14. shows that CHF_3 can produce not only better selectivity, but also a faster etching rate for SiO_2 than that of CF_4 with H_2. It also suggests that the etching mechanism in CHF_3 may be different from that in CF_4 vs. H_2.

In Table 5.2.3, the best selectivity of polysilicon to SiO_2 , Ta and Ta_2O_5 is in the etching gas of SF_6 adding Ar and the etching rate of poly in SF_6 is larger than that in CF_4. The result of selectivity shows that the etching gas of SF_6 adding Ar should be chosen if a poly gate will be etched on the top of either SiO_2 and Ta_2O_5. That the polymer is formed and deposited on the film to resist the etching in CF_4 should be the reason of higher etching rate of poly in SF_6. This table also shows that adding H_2 into SF_6 can decrease the etching rates of both SiO_2 and polysilicon because the hydrogen atom can form HF to reduce the concentration of fluorine radicals.

Table 5.2.2. RIE etch rate of poly, SiO_2 and Ta_2O_5 in CHF_3 and CF_4 with O_2 and H_2 of 30% fractions

Ratio(%O2,H2)	SiO2 (A/min)	Polysilicon(A/min)	Ta2O5 (A/min)
CF4+30%H2	199	105	48
CF4+20%H2	282	187	45
CF4+10%H2	324	185	55
CF4	408	237	116
CF4+6%O2	397	266	95
CF4+8%O2	411	255	118
CF4+15%O2	381	230	93
CF4+20%O2	381	259	117
CF4+25%O2	363	184	109
CF4+30%O2	279	157	77
CHF3	435	96	72

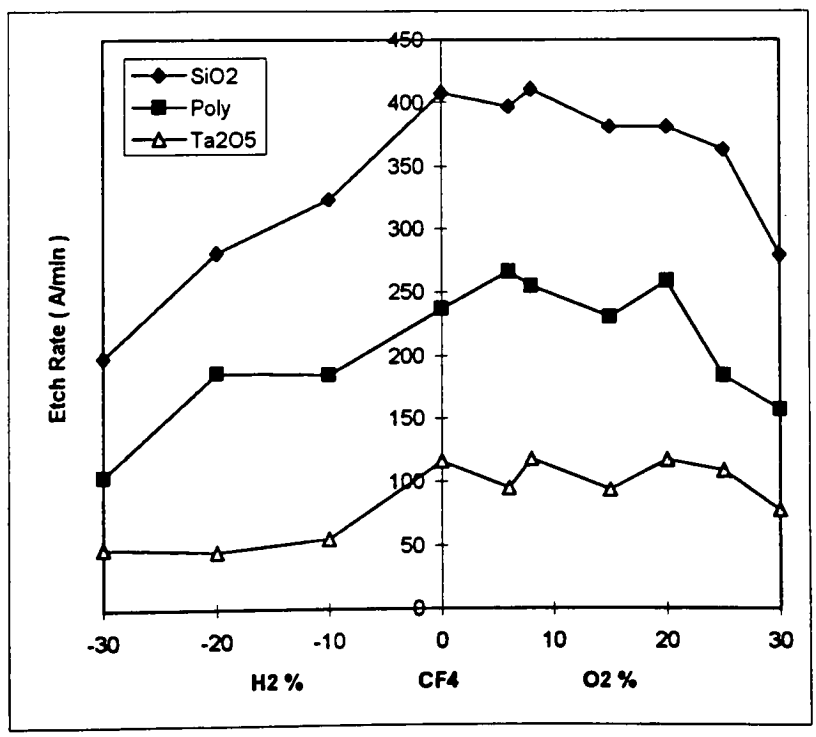


Fig. 5.2.13. Etch rates of RIE in CF_4 with O_2 and H_2

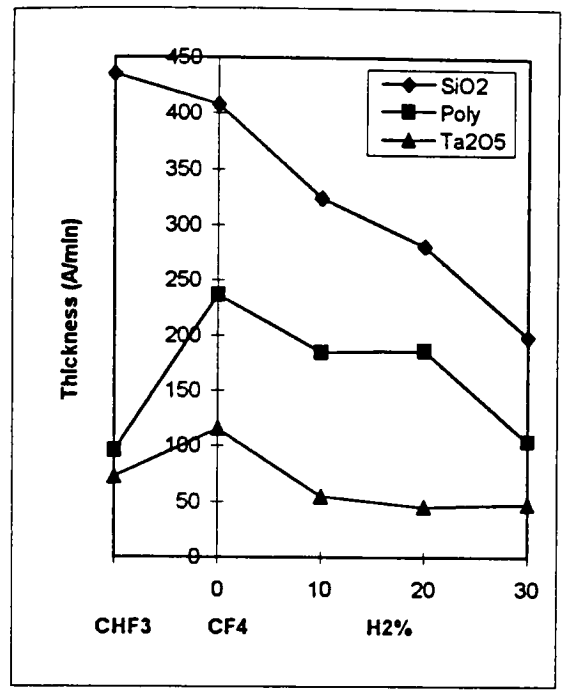


Fig. 5.2.14. RIE etch rate of CF_4 with H_2 % compared to pure CHF_3

Table 5.2.3. RIE etch rates of poly, Ta, Ta_2O_5, and SiO_2 in SF_6 with 20% fraction of Ar and H_2

	Power=150W		RIE Etch	Rate	(A/min)	
Gas	Flow Rate(sccm)	Pressure(mTorr)	Ta2O5	Ta	SiO2	Poly
SF6	50	80	240		440	5200
SF6	150	80	280		670	5200
SF6	150	200	45		105	3800
SF6:H2=0.8:0.2	50	80	60		350	2600
SF6:H2=0.8:0.2	150	80	250		450	2600
SF6:H2=0.8:0.2	150	200	40		220	2600
SF6:Ar=0.8:0.2	50	120	150	500	500	5200
SF6:Ar=0.8:0.2	150	120	250	1700	530	7500
SF6:Ar=0.8:0.2	150	200	110	1500	320	7500

Reference

[1] J. Grossman and D.S. Herman, " A new etchant for thin films of tantalum and tantalum compounda," J. Electrochem. Soc., vol.116, pp.674-674, 1969.

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Chapter 6. Conclusions and Future Studies

6.1 Summary

The two-step process, consisting two separate depositions and annealings, is successful in obtaining good quality Ta_2O_5 films with a high dielectric constant, high breakdown voltage, and low leakage current. The as-deposited Ta_2O_5 film is in the amorphous state while the annealed Ta_2O_5 film is in the crystalline state. The refractive index, dielectric constant, and density increase after annealing. There is an interface layer between silicon substrate and bulk Ta_2O_5 film, which can be condensed more than the bulk film during annealing. The second layer of Ta_2O_5 film deposited on an annealed Ta_2O_5 film can be more condensed than the film directly deposited on silicon substrate.

Apparent capacitance and leakage current of capacitor made of Ta_2O_5 film as dielectric layer is very sensitive to the substrate. A capacitor with an n-type silicon as the substrate has the smallest apparent capacitance and the highest leakage current. A capacitor with an n+-type substrate has normal capacitance and less leakage current. The capacitor with a p-type substrate has normal capacitance and the smallest leakage current. These results predict that the capacitor of Ta_2O_5 film with p+-type substrate will has the best electrical properties.

Wet etching using hot KOH solution is not suitable for Ta and Ta_2O_5 films on the silicon substrate due to the chemical cell effect between Ta or Ta_2O_5 film and silicon.

The RIE studies show that the best selectivity of polysilicon to SiO_2, Ta, and Ta_2O_5 is obtained with an etching gas of SF_6 with Ar addition. It is proposed that the

etching rate of polysilicon in SF_6 is larger than that in CF_4 because the CF_4 can be decomposed to form a polymer on the film surface which resists etching. Adding H_2 into SF_6 can decrease the etching rates of both SiO_2 and ploysilicon because the hydrogen atom can form HF to reduce the concentration of fluorine radicals. The lowest etching rate of Ta_2O_5 in CF_4 with addition of oxygen or hydrogen suggests that the surface reaction rates of tantalum oxide under this condition is primarily chemical with less bombardment.

There are two energy levels, 5.7 eV and 3.0 eV of crystal field, respectively, in Ta_2O_5 films. The energy level of 5.7 eV has stronger absorbency than that of 3.0 eV in uv-vis spectrum. There are two kinds of defects, a free volume-like defect and an oxygen vacancy-like defect, in Ta_2O_5 films. The free volume-like defect can split the 3.0 eV peak into 3.0 eV main peak and 2.4 eV peak in as-deposited Ta_2O_5 films. The oxygen vacancy-like defect can split the 5.7 eV peak into 5.7 eV main peak and 4.3 eV peak. During annealing, the oxygen vacancy-like defects increase and increase the absorbency spectrum, however, the free volume-like defect is released from the film and its absorbency disappears.

6.2. Future Work

As discussed in Chapter 3, the result predicts that the capacitor with p+-type silicon substrate could have the lowest leakage current. Further work could use p+-type substrate to make capacitors with the smallest leakage current.

The two-step process is able to make low leakage current and high dielectric constant Ta_2O_5 films. Further work could use the two-step process to make DRAM,s.

In the study of optic property, there was only one thickness of Ta_2O_5 film. The change of absorbency spectrum with sample thickness and different substrates should be investigated to determine the effect of interface and thickness on absorbency spectrum.

Tantalum Oxide Thin Films for Microelectronic Applications

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Abstract

Over the last several years, tantalum pentoxide (Ta2O5) thin films have received much attention as chip integrated high permittivity, high breakdown strength dielectric for storage capacitors for ULSI DRAMs. We have studied the properties of reactively sputtered films of Ta2O5 on silicon wafers. These films have been characterized for refractive index. X-ray diffraction studies on films annealed in oxygen ambient at 800C show the films to crystallize into an orthorhombic phase with an increase in refractive index to the bulk value. Various capacitor configurations such as MIM, MIS (on p-type and n-type Si substrates) have been fabricated to study the nature of Ta2O5/Si interface. The capacitors fabricated on p-type Si exhibit lower leakage. The reactive ion etching behavior of Ta2O5 is investigated in CF4 + O2 and CHF3. It is observed that these films show lower etch rate as compared to Si and SiO2, however in CHF3 the etch rates of Si and Ta2O5 are comparable.

1. Introduction

There is a critical demand for new dielectric films having higher dielectric constants, higher dielectric strengths and low leakage currents for applications such as a) charge storage capacitors for memory cells in ULSI DRAMs [1-2], and b) low-inductance decoupling capacitors for the control of simultaneous switching noise (SSN) in high-speed switching ULSI chips [3-4].

Among these new insulators, tantalum pentoxide has received considerable attention. Several papers have been reported on the electrical properties of Ta2O5 films grown by various techniques [5-6]. It has been reported that the electrical properties e.g. dielectric constant, leakage current, dielectric strength as well as the nature of Ta2O5/Si interface is extremely sensitive to the annealing conditions [7]. At present, however the role of as deposited Ta2O5/ Si interface is not fully understood. We have studied I-V and high frequency (1 MHz) C-V characteristics of Al/Ta2O5/Al, Al/Ta2O5/p-Si and Al/Ta2O5/n-Si capacitors.

In order to integrate this dielectric into silicon technology, it is essential to explore dry etching processes to selectively etch Ta2O5 films on SiO2 and Si surfaces. The selectivity of Ta2O5 to Ta has been studied using reactive ion etching in CF4 and CHF3 [8]. However, no such study is available on the selectivity of Ta2O5 to silicon or silicon dioxide. We have studied the etching rates of Ta_2O_5 in CHF3 and CF4 with varying amounts of O2, and compared with those of LPCVD deposited polysilicon and thermally grown SiO2.

2. Experimental

The tantalum oxide films were deposited on Si wafers by reactive DC sputtering from an 8" diameter Ta target in Ar with 20 % oxygen. The films were sputtered at a pressure of 5 mTorr and a DC power of 700W. The deposition rate of 2.5 nm/min was generally obtained at these conditions. The films were characterized for thickness and refractive index using an ellipsometer. The film phase was identified using an X-Ray diffractometer (Rigaku DMAX B) employing Cu K-alpha radiation.

Metal-insulator-semiconductor (MIS), and metal-insulator-metal (MIM) capacitors with Al electrodes were fabricated using lithography and wet

etching. The area of Al gate ranged from 0.4 to 2.0 square mm. The I-V and C-V measurements were made using HP 4145 parameter analyzer and HP 4275 A LCR meter, respectively.

The RIE selectivity of Ta2O5 to Si and SiO2 was studied using the plasma gas compositions from pure CHF3 to CF4 with different fraction of O2 up to 30 %. The RIE parameters used were: power: 150 W; pressure: 20 mTorr; flow rate 50 sccm. For accurate comparison of various etch rates, large regions of Ta2O5 film (130 nm), LPCVD polysilicon (500 nm), and thermal SiO2 (500 nm) were defined on 4 " diameter wafers using sequential lithography. The change in thickness of each region following a particular RIE treatment was determined using optical thickness measurement instrument: Nanospec /AFT 010-0180.

3. Results and Discussions

3.1 Physical Property

As deposited films of Ta2O5 have been reported earlier to be amorphous [7]. An annealing at temperatures above 750 C is required to crystallize reactively sputtered films of Ta2O5. Figure 1 shows an XRD pattern of a film annealed at 800 C for 30 minutes in oxygen, confirming the existence of orthorhombic Ta2O5 phase (ASTM 8-255)

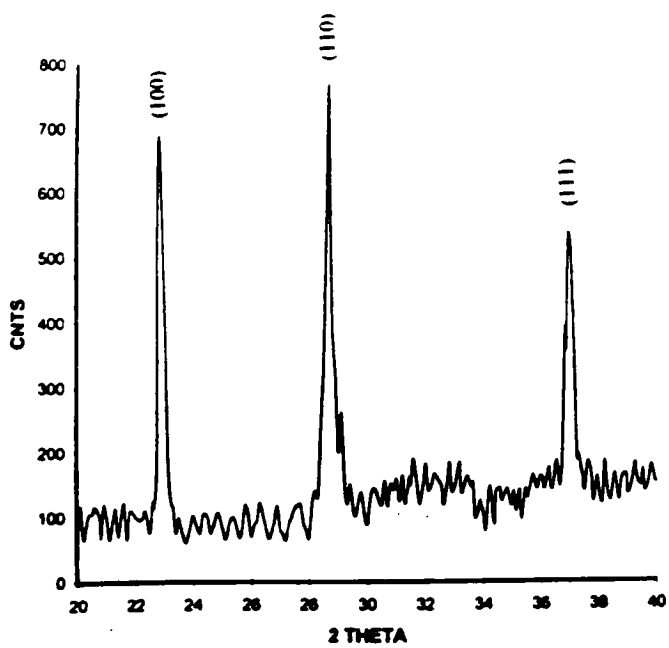

Figure 1. X-ray diffraction pattern of the Ta2O5 annealed at 800 C, 30 min. in oxygen.

The refractive index measured on Ta2O5 films on Si wafers is found to be generally lower in thin films (30 nm). This indicates that the film may not be continuous in the initial stages of deposition. A lower deposition rate may be necessary for thin films.

3.2 Electrical Properties

For the measurement of leakage current , I-V curves were plotted. The typical characteristics for Al/20 nm Ta2O5/ p-Si for Al/40 nm Ta2O5/ n-Si capacitors are shown in Figures 2 and 3 respectively. It is apparent that the type of the semiconductor has a significant influence on the leakage currents. The films on p-type Si substrate can sustain an electric field of 3 MV/cm at a current density of 1 uA/cm2 in the accumulation mode. which is an order higher than that observed in films on n- type substrate. It is also observed that the devices on p-type substrate give higher leakage current in the depletion-inversion mode whereas the devices on n-type substrate are found to be more leaky in the accumulation mode. Under both situations, electrons are adjacent to the interface. It is also known that as deposited Ta2O5 films are oxygen deficient [9] and therefore electrons transport may contribute to excessive leakage. Several investigations on annealing of these films in oxidizing ambients such as oxygen and ozone have shown improvements in leakage currents [7, 10]

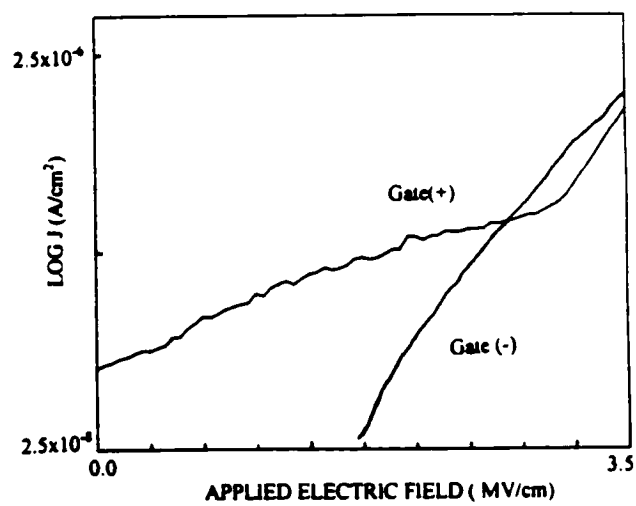

Figure 2. Leakage current density -applied field characteristics for Al/20 nm Ta2O5/ p-Si capacitor.

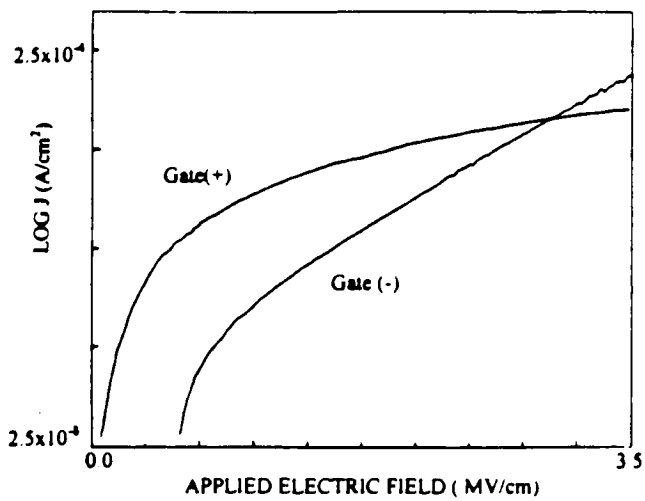

Figure 3. Leakage current density -applied field characteristics for Al/40 nm Ta2O5/ n-Si capacitor.

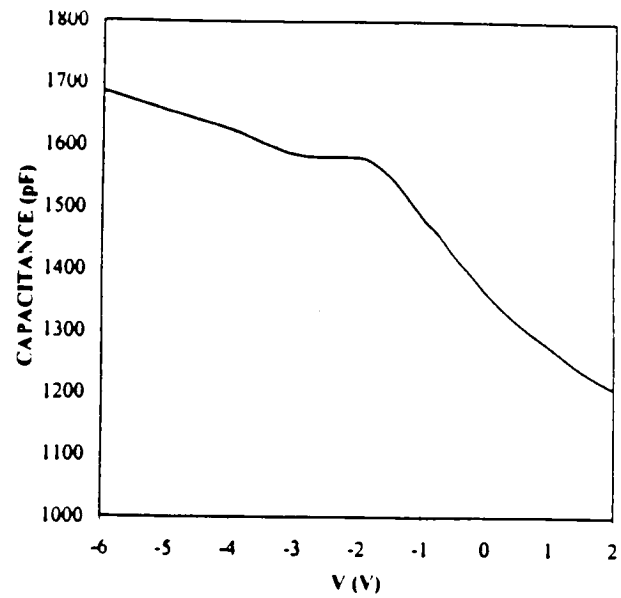

Figure 4. C-V characteristics for Al/20 nm Ta2O5/p-Si capacitor with area 4E-3 cm^2 at 1MHz.

Figures 4 and 5 show typical C-V curves for Al/20 nm Ta2O5/ p-Si and Al/40 nm Ta2O5/ n-Si measured at 1 MHz, respectively. The capacitance values have been corrected for the parasitic series resistance. The value of apparent dielectric constant estimated from the oxide capacitance varies from 6 to 10 in films deposited on silicon. However, in Al/ Ta2O5/Al structures, it is found to be higher 16. These values are considerably smaller than 23 observed in bulk Ta2O5. It must be noted that theses films are unannealed and are not dense enough.

A flat band voltage of -0.6 V is calculated for capacitors on n-Si with substrate doping of 7E14 cm^{-3} from which total oxide trap density Qit/q = 1.3 E11 cm^{-2} is estimated. Similar analysis could not be done on devices on p-substrate.

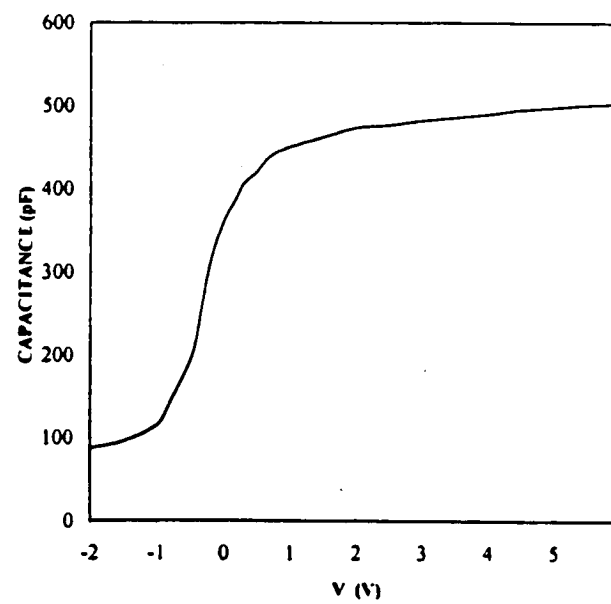

Figure 5. C-V characteristics for Al/40 nm TaO5/n-Si capacitor with area 4E-3 cm^2 at 1 MHz

3 3 Reactive Ion Etching

The etch rates of Ta2O5, polysilicon and SiO2 for different gas compositions were computed and are shown in Figure 6. It is observed that Ta2O5 etches slowest with an average etch rate of 10 nm/min in CF4 with O2 fraction up to 25 % while poly-Si and SiO2 etch considerably faster. However, in CHF3 ambient, the etch rate of poly-Si decreases sharply and almost approaches that of Ta2O5.

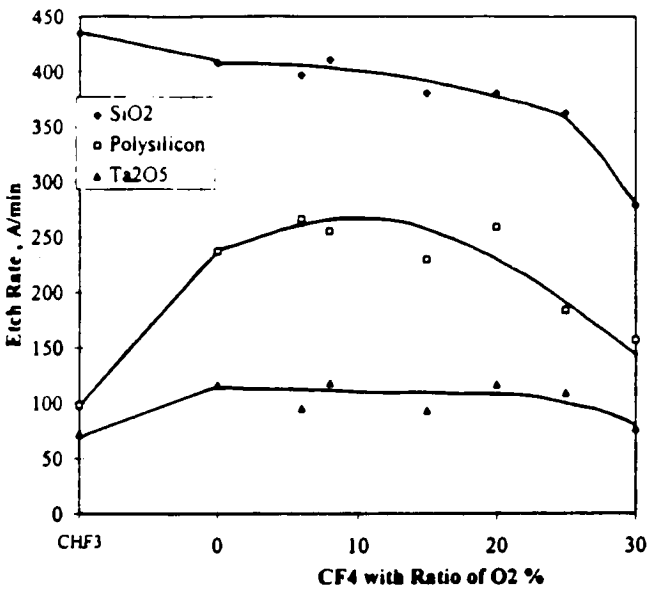

Figure 6. Reactive ion etch rates of SiO2, polysilicon and Ta2O5 in CHF3, and CF4 + O2 at a power of 150 W, pressure 20 mTorr, and flow rate 50 sccm.

This suggests that the surface reaction rates of tantalum oxide under this condition which is primarily chemical with less bombardment are much slower than those of Si and SiO2. By exchanging one F atom in the CF4 molecule with one H atom, the etching of Si is suppressed. This has been explained in terms of more accumulation of non volatile residue (carbon residue) on non oxide surfaces such as Si [11]. On the other hand the etching of SiO2 continues. The decrease in etch rate of Ta2O5 in CHF3 has been discussed due to the formation of higher fluorinated organic layer on CHF3 etched surfaces [8]. This indicates that with incorporation of hydrogen in CF4, a desired selectivity may be obtained. These studies are currently under investigation.

Summary

The properties of reactively sputtered Ta2O5 films are extremely sensitive to the nature of substrate, in particular, to the semiconductor type. The etching selectivity of Ta2O5 may be obtained in hydrogen containing CF4, which is currently under investigation.

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